SuperSpeed USB 3.0 Technology Overview and Industry Update

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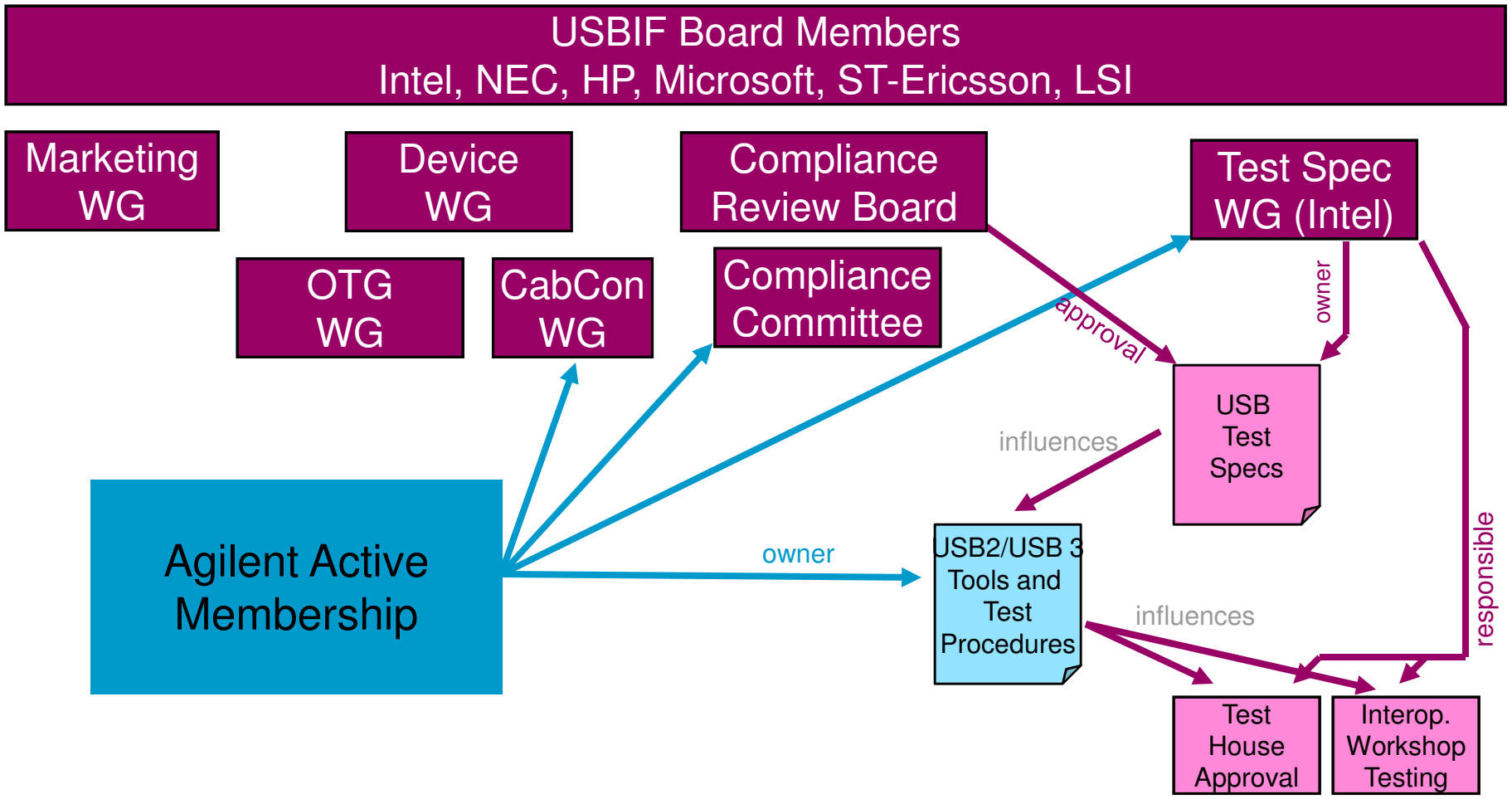
USB Product Manager
Agilent Technologies

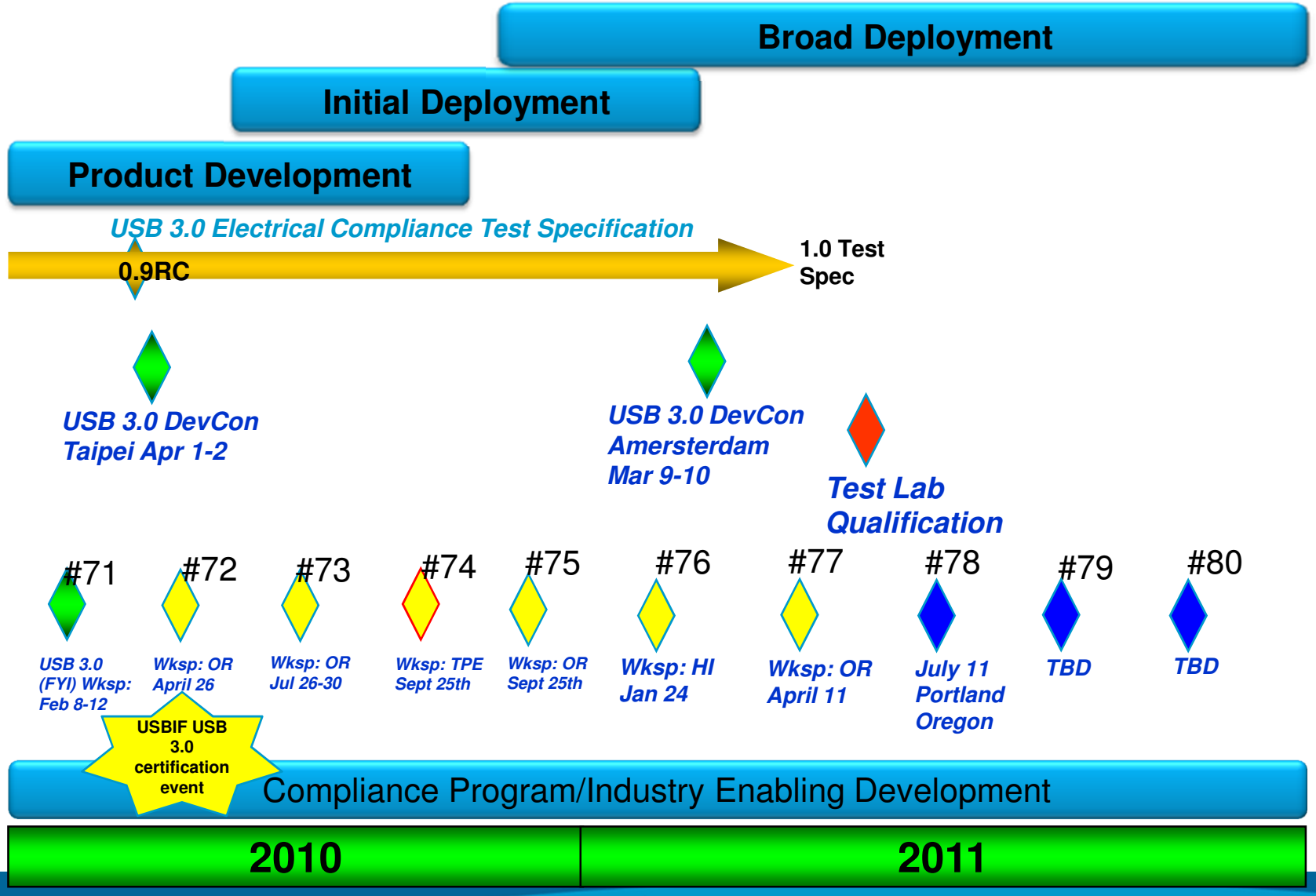
Agenda

- ❑ Introduction
- ❑ USB 3.0 Industry Overview
- ❑ Physical Layer Overview
- ❑ Physical Layer Testing
- ❑ Cable and Connector Testing
- ❑ Compliance Test Challenges
- ❑ Thunderbolt?
- ❑ Precision Probe
- ❑ Questions

USB Implementors Forum, inc (USB-IF)



SuperSpeed USB Timeline



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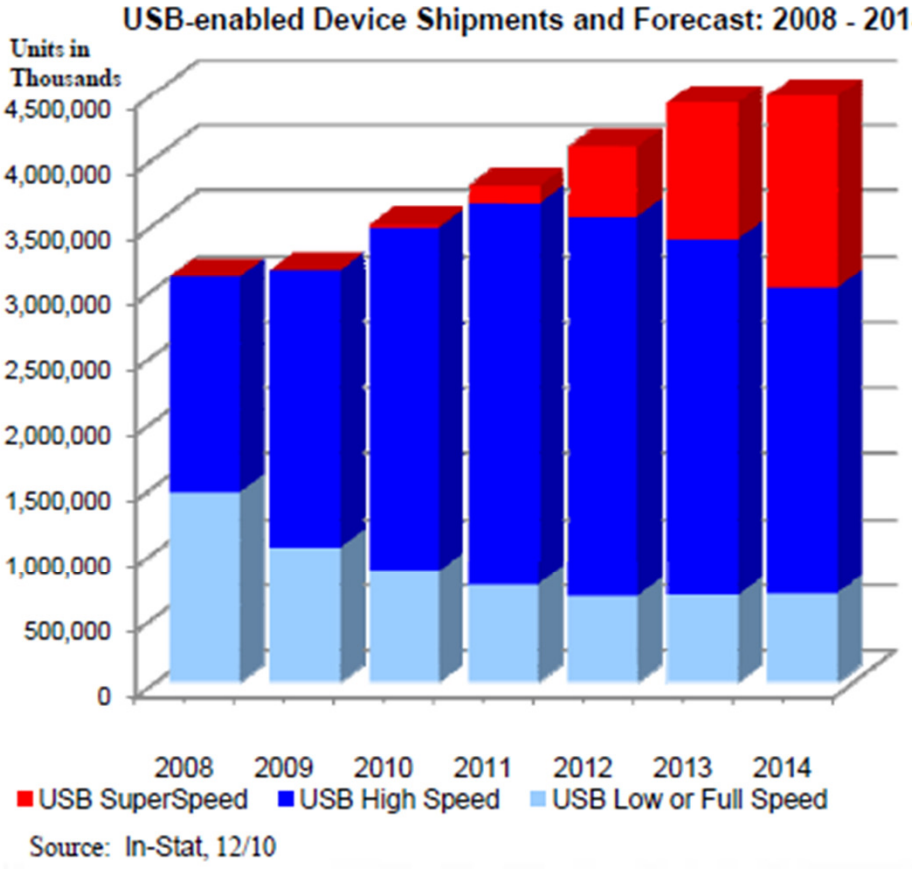
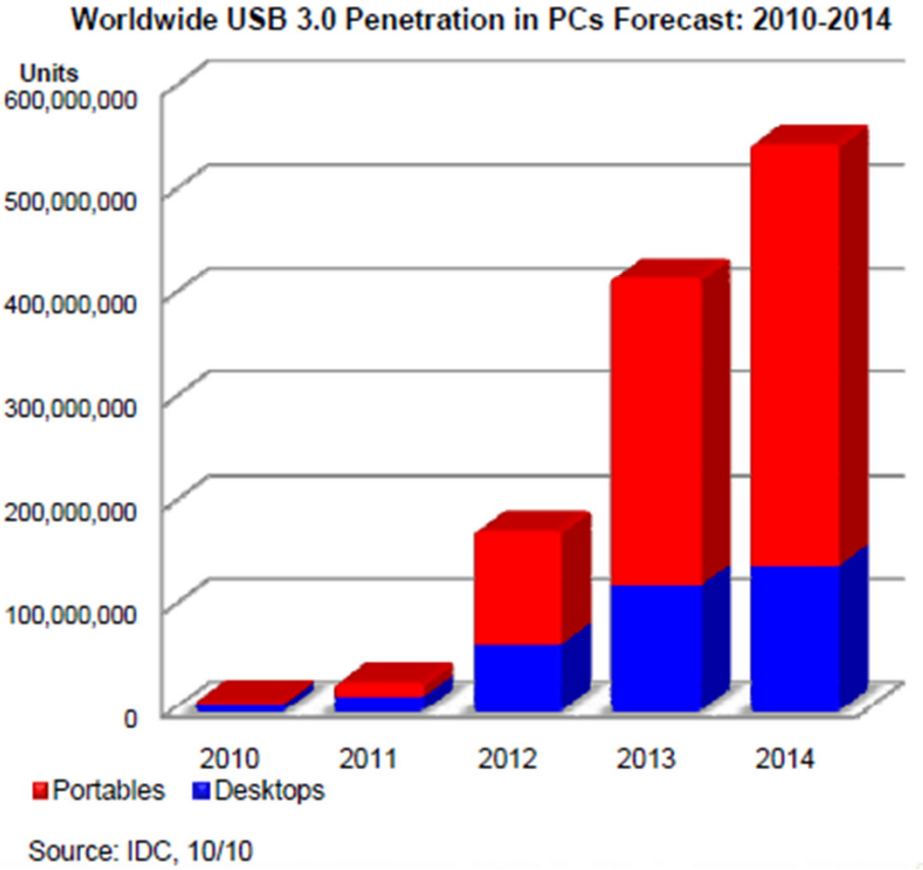
SuperSpeed USB 3.0 Key Messages

- SuperSpeed USB is in the broad adoption phase!
  - Over 230 Certified SuperSpeed USB 3.0 Products
    - 10 host Silicon, 8 IP building blocks, 49 Peripheral Silicon, 73 Peripherals and 97 Systems!
    - https://www.usb.org/kcompliance/ilist
- 21+ Million USB 3.0 Host Controllers shipped in 2010.
  - USBIF estimates much greater than 60 Million by EOY 2011
  - http://www.usb.org/developers/presentations/ to download DevCon slides from March of this year.

Worldwide shipment of USB-enabled Devices



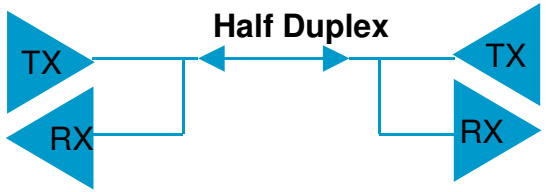


- USB install base is 10+ billion and growing at 3+ billion a year.

USB 3.0 Physical Layer Test Challenges

•USB 2.0 High-Speed

- ✓ 480Mbps
- ✓ NRZI, Half Duplex
- ✓ 4 signals
  Dp, Dm, VCC, GND
- ✓ Cable Lmax= 5meter
- ✓ $I_{configLP/FP}$ = 100mA/500mA
- ✓ $I_{suspend}$ = 500uA
- ✓ No SSC
- ✓ TX SQ at Near End
- ✓ No Host RX testing

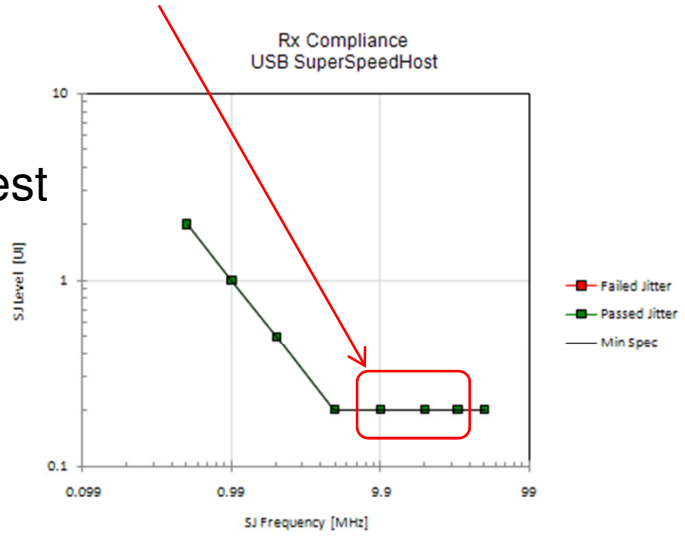


•USB 3.0 SuperSpeed

- ✓5 Gbps
- ✓8B/10B PRBS, Full Simplex
- ✓8 signals
  4 USB2 , 4 SS Signals
- ✓Cable L_{max}= 3 meters
- ✓$I_{configLP/FP}$ = 150mA/900mA
- ✓$I_{suspend}$ = 2.5mA
- ✓SSC
- ✓TX at End of Channel (Far end)
- ✓RX Jitter tolerance

0.9 Draft, USB 3.0 PHY Electrical Test Specification

- Key Updates
  - RX compliance calibration and testing performed at end of the channel
  - Channel definition of 3 meter cable plus 5” trace for host and 11” trace for Device
  - Separate calibrations performed for device and host testing with specific device or host test fixtures
  - Addition compliance Pj test points defined at 10Mhz, 20Mhz and 33Mhz
  - TX testing will requires channel embedding
    - Golden s-parameters selected for embedded test
  - Device RX eye calibration set to 145mVpp
  - Host RX eye calibration set to 180mVpp



USB 3.0 Compliance Test Matrix

USB 3.0 Product Test Matrix

		USB 3.0 xHCI /SuperSpeed Testing									USB 2.0 LS/FS/HS Testing			
		USBCV Chap 9 Tests	USBCV Device Specific Tests	xHCI Host Tests	3.0 Electrical	3.0 Interop	3.0 Backwards Compat-ibility	Link Testing	xHCI HSET	Current Test Measure ment	USBCV Chap 9	USBCV Device Specific Tests	2.0 Gold Tree Interop using EHCI	2.0 Electrical
xHCI Host	Silicon	x	n/a	Full test suite	x	x	x	x	x	?	All speeds	All	n/a	x
	End Product	x	n/a	Subset	x	x	x	x	x	?	All speeds	All	n/a	x
USB 3.0 Devices Silicon/IP/End Product	Device	x	n/a	n/a	x	x	x	x	x	x	Run for all 2.0 supported speeds	n/a	x	x
	Hub	x	Hub tests	n/a	On both upstream and downstream ports	x	x	x	x	x	Run for all 2.0 supported speeds	Hub Tests	x	x
	MSD Device	x	MSD tests	n/a	x	x	x	x	x	x	Run for all 2.0 supported speeds	MSD Tests	x	x

Test Notes:	
	Subset of xHCI tests: register interface tests, port speed and port tests, 1 Isoch, bulk, control interrupt loopback on 1 port
	Until we have a 3.0 certified hub, substitute various 3.0 devices being swapped in and out for 3.0 interop
	3.0 Electricals on Agilent, LeCroy and Tek using external BERT
	xHCI Host USB 3.0 CV chap 9 for these devices: 2.0 hub, 3.0 hub, SS/HS/FS/LS devices

USBIF source at http://www.usb.org/developers/ssusb/ssusb_pil/USB_3_0_Test_Matrix.pdf

USB-IF Still Provides USB 3.0 Certification at Intel PIL – Focus is on Hosts and Hubs

Tech Bulletin

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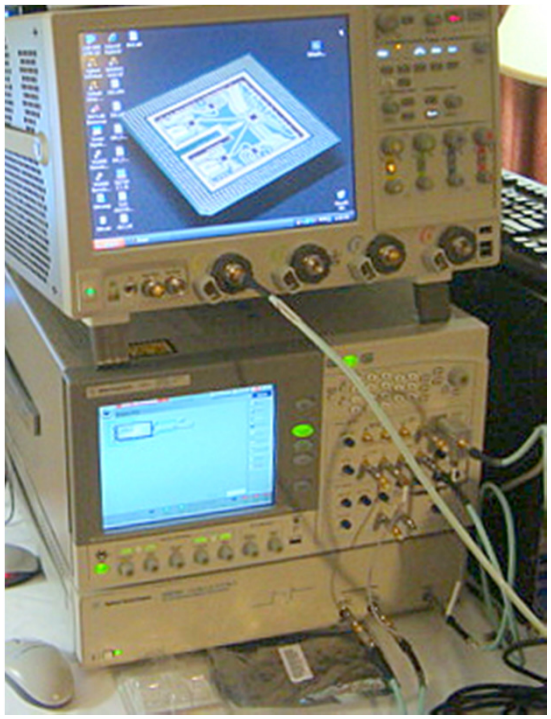
USB-IF Launches SuperSpeed USB Platform Interoperability Lab

CEBIT, Hanover, Germany – March 3, 2009 – The USB Implementers Forum (USB-IF) today announced the availability of the SuperSpeed USB Platform Interoperability Lab (PIL), providing USB 3.0 developers the opportunity to test host and device interoperability and ensure that devices perform correct USB 3.0 electrical signaling and link level transactions. Additionally, the lab will test conformance to the Framework defined in the USB 3.0 specification. The PIL will provide USB technology expertise to early host/device manufacturers as well as platforms with early implementations of host and device components for performing interoperability testing.

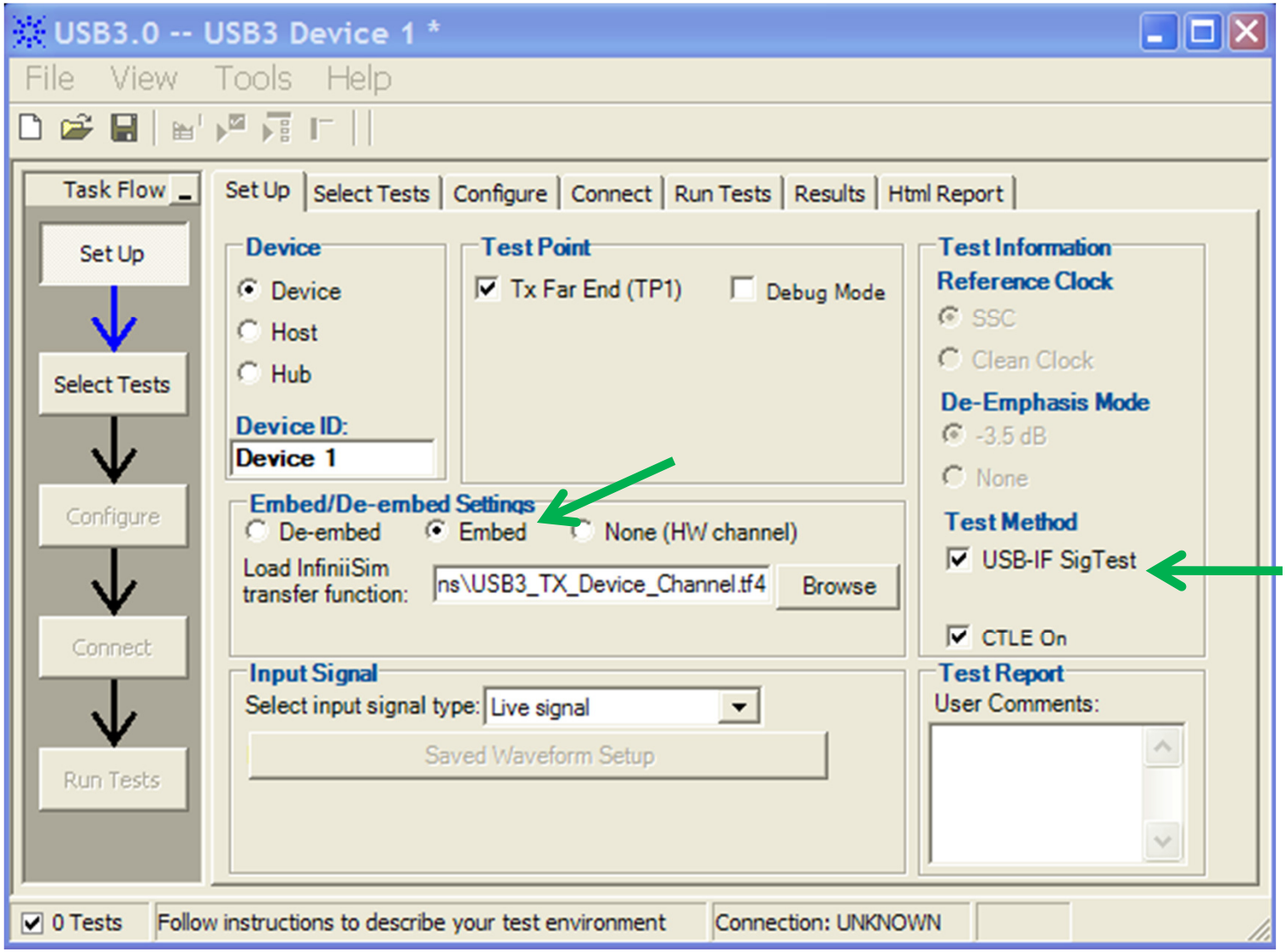


- PIL still performing testing between USBIF workshops
- Test lab expected to start certification soon.

- http://www.usb.org/developers/ssusb/ssusb_pil

Testing will be completed per the following USB 3.0 Product Test Matrix.

U7243A USB 3.0 TX Compliance Application



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Transmitter test requirements

The eye diagrams are to be measured into 50-Ω single-ended loads.

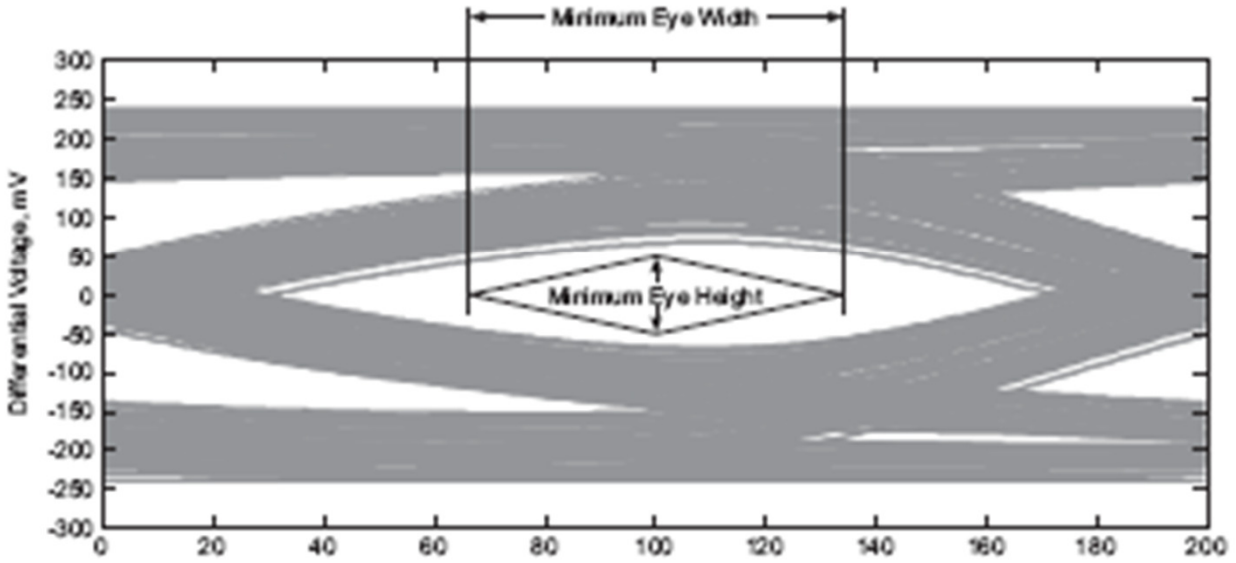
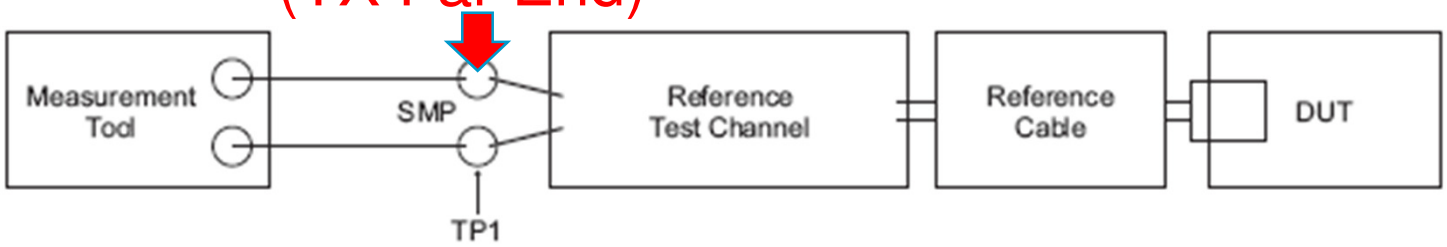


Table 6-12. Normative Transmitter Eye Mask at Test Point TP1

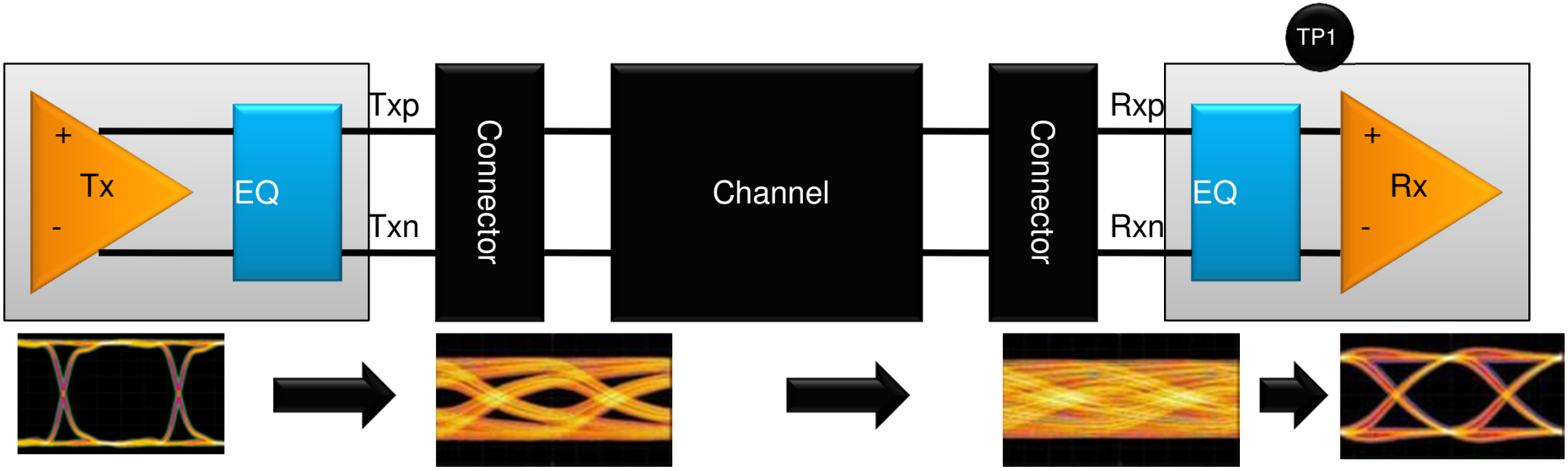
Signal Characteristic	Minimal	Nominal	Maximum	Units	Note
Eye Height	100		1200	mV	2, 4
Dj			0.43	UI	1,2,3
Rj			0.23	UI	1,2,3, 5
Tj			0.66	UI	1,2,3

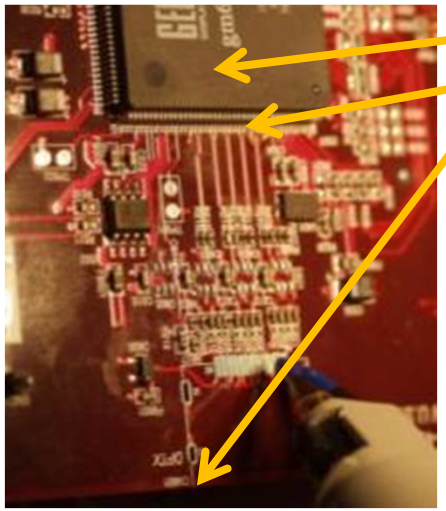
(TX Far End)



USB 3.0 Signal Path Flow

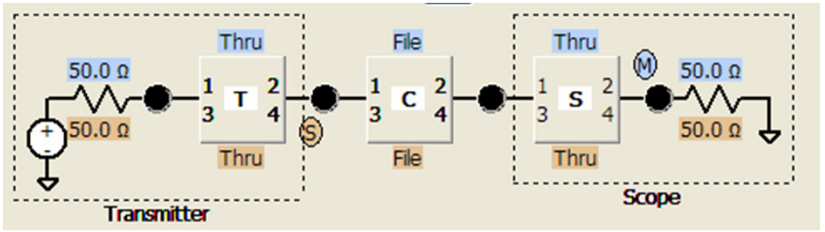
USB 3.0 Specification defines TP1
As the measurement location





Signal generated here
Exits IC here
Exits board here

Combine measurements and transmission line models to view simulated scope measurements at any location in your design



Load S-Parameters into Signal Path

S-Parameters

m100223a_DemBd54916_26408v5sn450_A_p1J16p2J17.s2p - Notepad

File Edit Format View Help

```
!Agilent Technologies,N5245A,MY49151035,A.08.60.09
!Agilent N5245A: A.08.60.09
!Date: Tuesday, February 23, 2010 18:18:08
!Correction: S11(Full 2 Port(1,2))
!S21(Full 2 Port(1,2))
!S12(Full 2 Port(1,2))
!S22(Full 2 Port(1,2))
!S2P File: Measurements: S11, S21, S12, S22:
# Hz S  dB   R 50
10000000 -1.224343e+001 -1.772934e+002 -4.689444e+000 -4.055600e+000
20000000 -1.221624e+001 1.791212e+002 -4.735650e+000 -5.167600e+000
30000000 -1.223820e+001 1.770460e+002 -4.753351e+000 -6.887907e+000
40000000 -1.224887e+001 1.752930e+002 -4.758249e+000 -8.748381e+000
50000000 -1.225741e+001 1.736047e+002 -4.773274e+000 -1.065208e+001
60000000 -1.229180e+001 1.720742e+002 -4.772188e+000 -1.257893e+001
70000000 -1.232777e+001 1.705868e+002 -4.775970e+000 -1.455881e+001
80000000 -1.235762e+001 1.691501e+002 -4.780704e+000 -1.653611e+001
90000000 -1.239385e+001 1.676880e+002 -4.787488e+000 -1.849432e+001
100000000 -1.243223e+001 1.662739e+002 -4.794525e+000 -2.045283e+001
110000000 -1.247415e+001 1.648788e+002 -4.802291e+000 -2.244328e+001
120000000 -1.251828e+001 1.634819e+002 -4.808766e+000 -2.442240e+001
130000000 -1.256693e+001 1.620814e+002 -4.814651e+000 -2.640366e+001
140000000 -1.262438e+001 1.607373e+002 -4.820703e+000 -2.839193e+001
150000000 -1.268803e+001 1.594424e+002 -4.828022e+000 -3.037498e+001
160000000 -1.274603e+001 1.581215e+002 -4.833044e+000 -3.234686e+001
170000000 -1.280791e+001 1.567978e+002 -4.840835e+000 -3.432754e+001
180000000 -1.287825e+001 1.554966e+002 -4.847504e+000 -3.631363e+001
190000000 -1.295092e+001 1.541922e+002 -4.852639e+000 -3.828690e+001
200000000 -1.302776e+001 1.529226e+002 -4.862398e+000 -4.026189e+001
210000000 -1.311045e+001 1.516999e+002 -4.866248e+000 -4.225240e+001
220000000 -1.319273e+001 1.504794e+002 -4.875292e+000 -4.422349e+001
230000000 -1.327862e+001 1.492515e+002 -4.883096e+000 -4.619004e+001
240000000 -1.337046e+001 1.480504e+002 -4.889324e+000 -4.814336e+001
250000000 -1.346412e+001 1.468278e+002 -4.896165e+000 -5.012396e+001
260000000 -1.356675e+001 1.456860e+002 -4.904943e+000 -5.208196e+001
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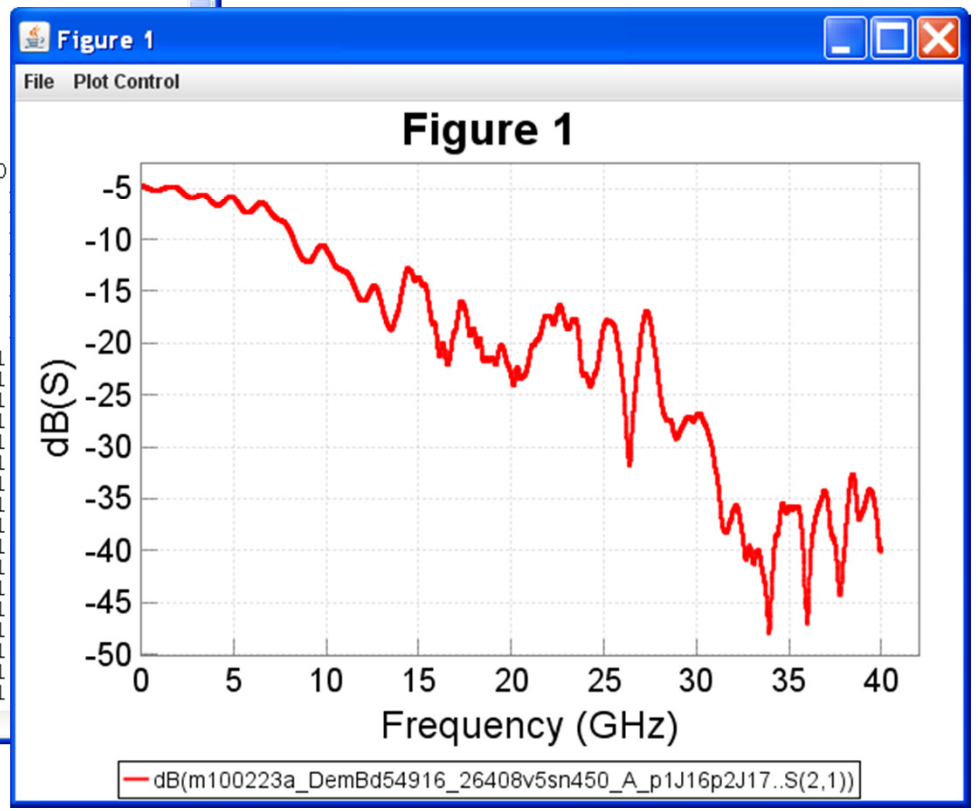
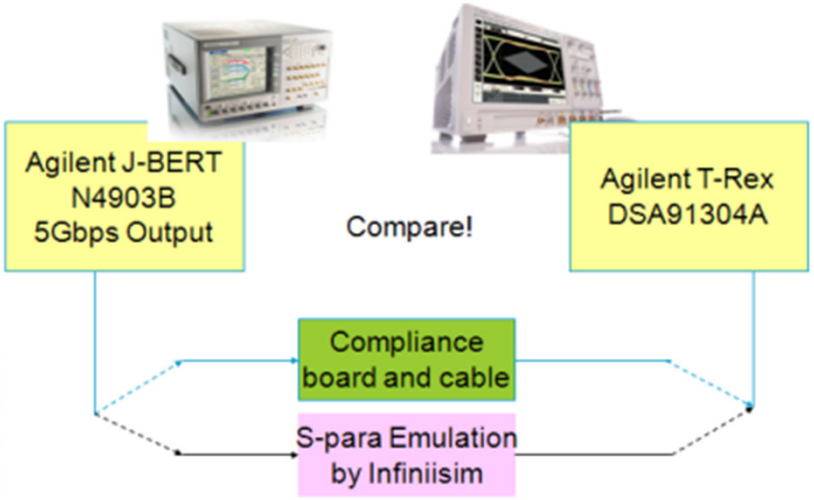
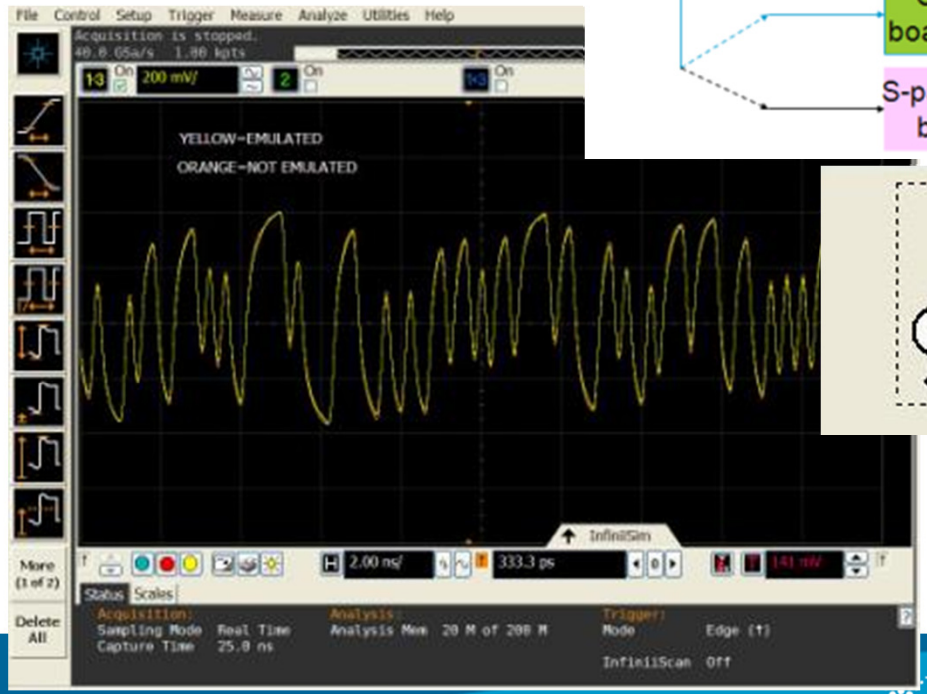


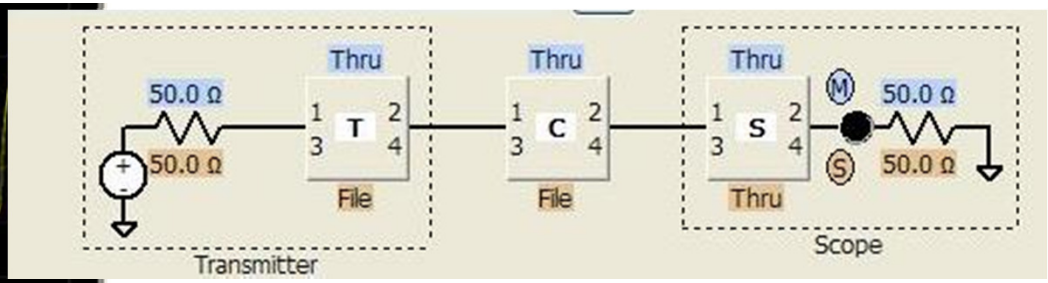
Plot showing S21 Insertion Loss

Tx testing emulated through s-parameters

Embed Channel File
"DEVICE_3MCABLE.s4p"



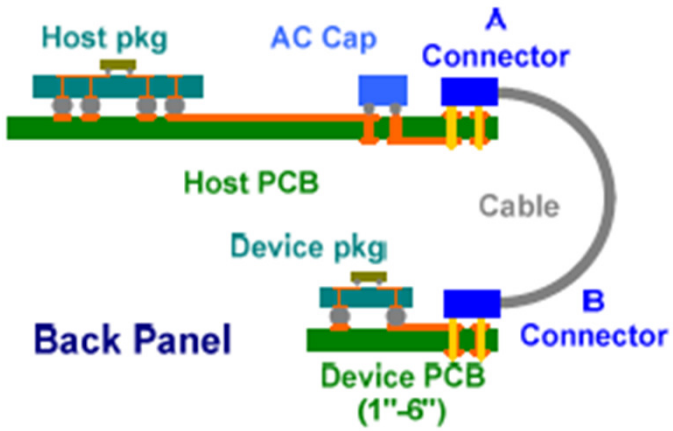




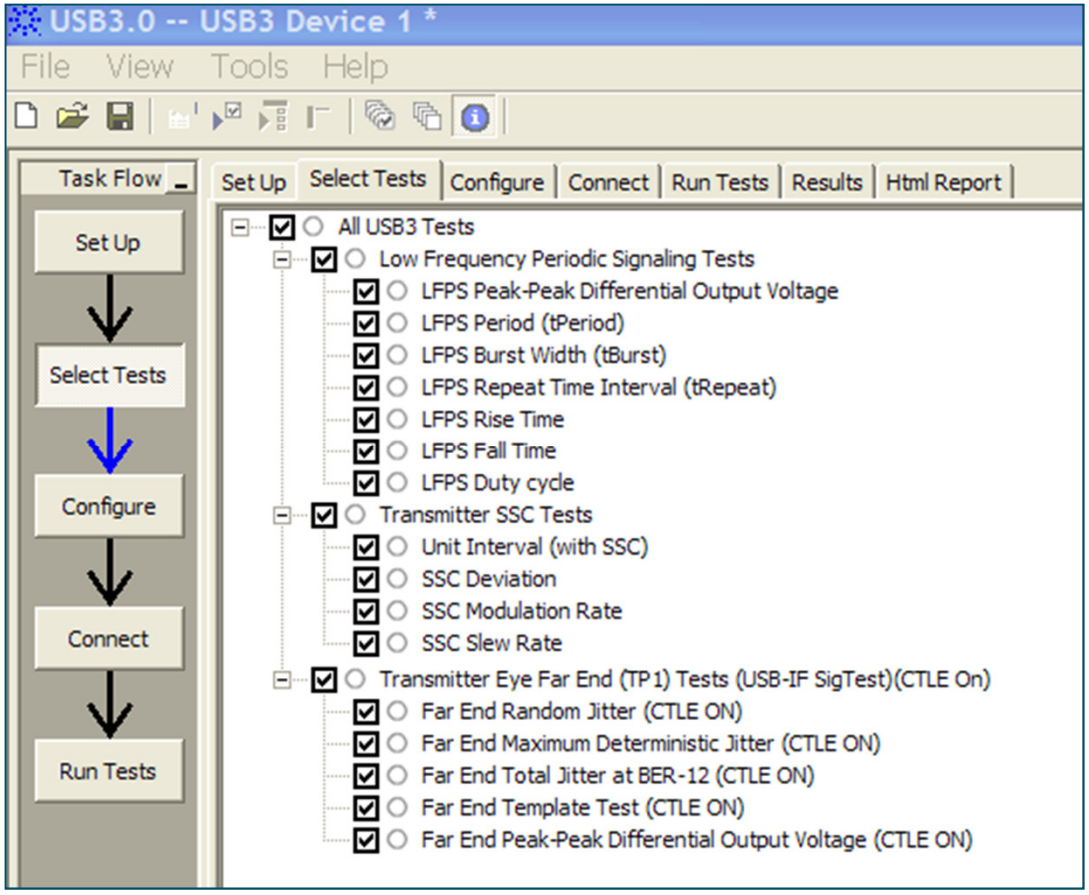
Validation with InfiniiSim of DSA91304A

Compliance Channels

- Compliance Channels are used to test TX and RX for worst case channel conditions
- Back panel USB route solution
  - Channel loss will dominate
  - Host 11” of trace
  - Device 5” of trace
  - 3 meter USB 3.0 cable



Transmitter Tests



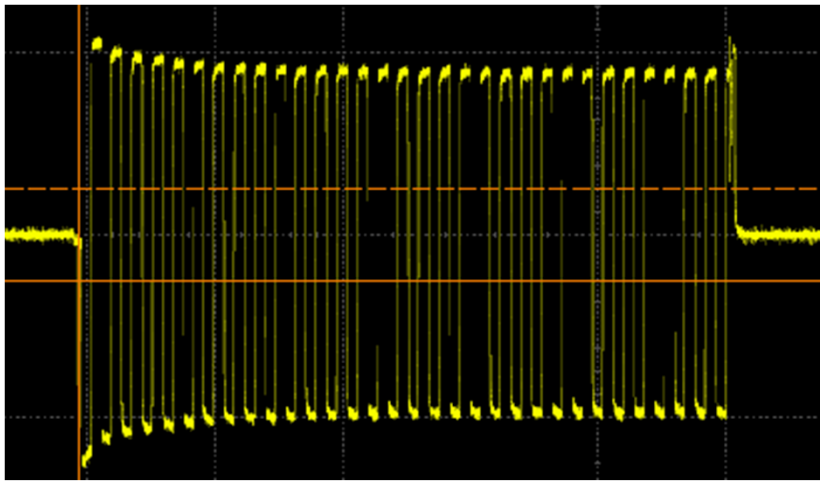
TX tests:

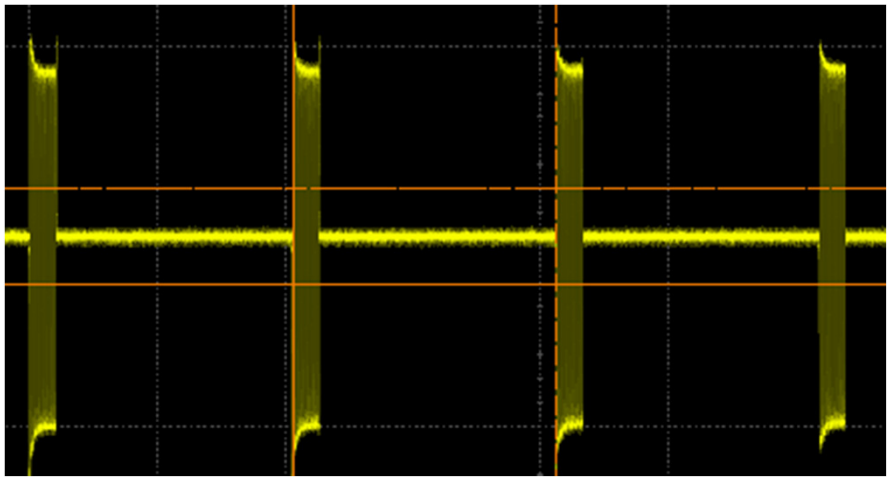
- LFPS (Near end)
- SSC (Near end)
- TX (Far End: TP1)
  - Eye Pattern
  - Tj, Dj (CP0 Pattern
  - Rj (CP1 Pattern)
  - Amplitude

"Embedded channel"

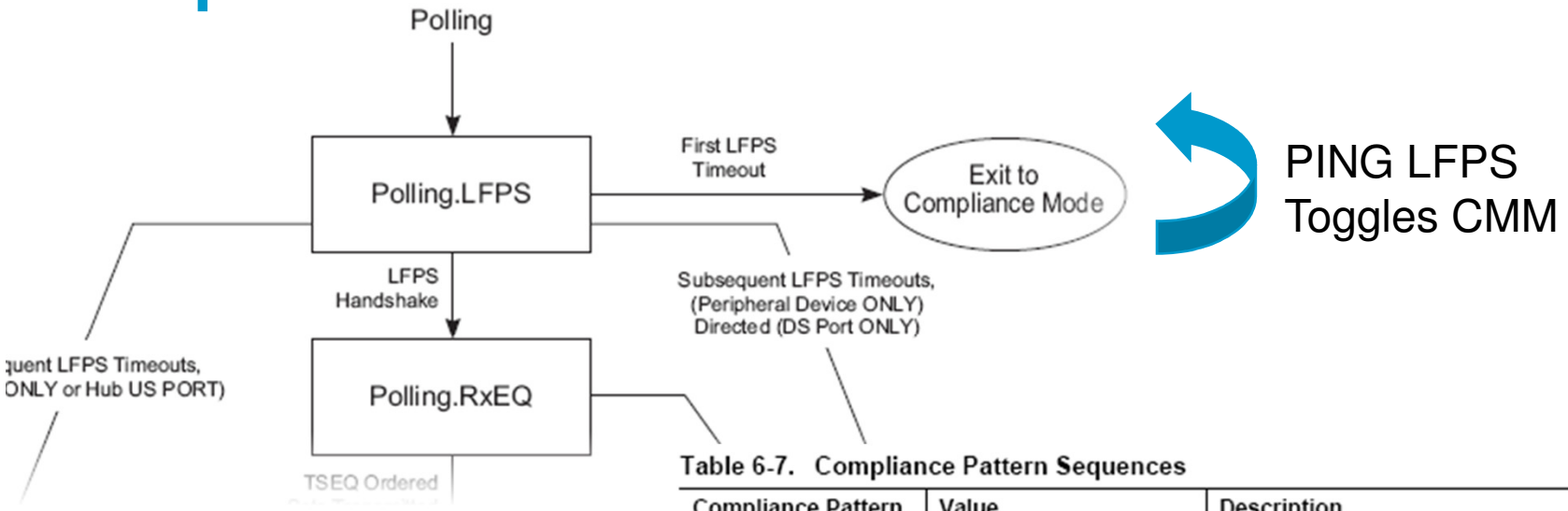
LFPS Test Requirements

Pass	# Failed	# Trials	Test Name	Worst Actual	Worst Margin	Spec Range
✓	0	1	LFPS Peak-Peak Differential Output Voltage	830.3mV	7.6 %	800.0mV <= VALUE <= 1.2000V
✓	0	1	LFPS Period (tPeriod)	32.0616ns	15.1 %	20.0000ns <= VALUE <= 100.0000ns
✓	0	1	LFPS Burst Width (tBurst)	1.0236µs	47.1 %	600.0ns <= VALUE <= 1.4000µs
✓	0	1	LFPS Repeat Time Interval (tRepeat)	10.3056µs	46.2 %	6.0000µs <= VALUE <= 14.0000µs
✓	0	1	LFPS Rise Time	387.2ps	90.3 %	VALUE <= 4.0000ns
✓	0	1	LFPS Fall Time	392.2ps	90.2 %	VALUE <= 4.0000ns
✓	0	1	LFPS Duty cycle	51.6350%	41.8 %	40.0000% <= VALUE <= 60.0000%





TX Testing Requirements: Polling.LFPS to compliance mode



PING LFPS
Toggles CMM

CP0
Dj

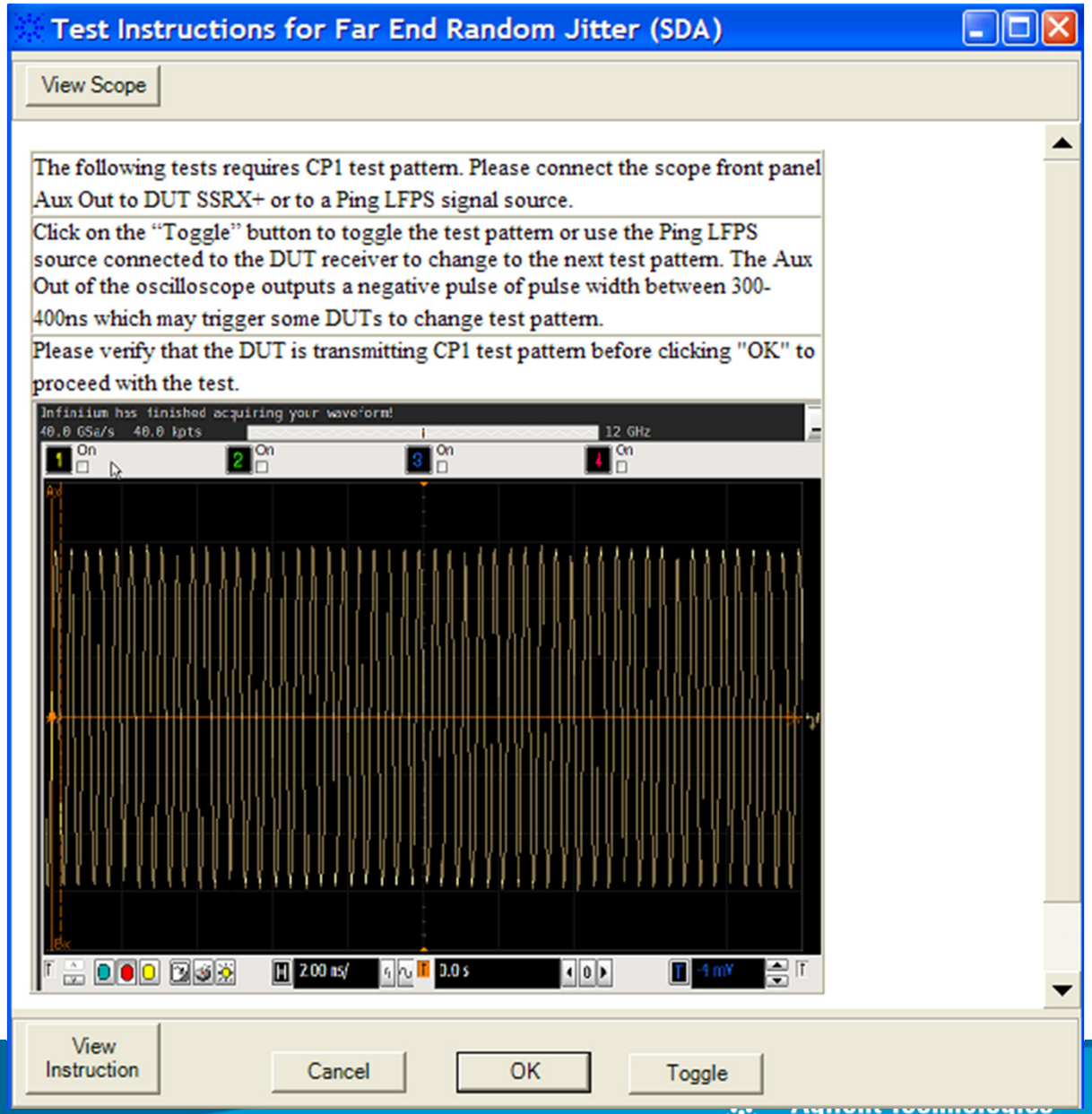
CP1
Rj

Table 6-7. Compliance Pattern Sequences

Compliance Pattern	Value	Description
CP0	D0.0 scrambled	A pseudo-random data pattern that is exactly the same as logical idle (refer to Chapter 7) but does not include SKP sequences
CP1	D10.2	Nyquist frequency
CP2	D24.3	Nyquist/2
CP3	K28.5	COM pattern
CP4	LFPS	The low frequency periodic signaling pattern
CP5	K28.7	With de-emphasis
CP6	K28.7	Without de-emphasis
CP7	50-250 1's and 0's	With de-emphasis. Repeating 50-250 1's and then 50-250 0's.
CP8	50-250 1's and 0's	With without de-emphasis. Repeating 50-250 1's and then 50-250 0's.

Note: Unless otherwise noted, scrambling is disabled for compliance patterns.

Toggling USB 3.0 TX test modes



•Connect Aux Out to DUT SSRX+ to toggle test modes

Transmitter testing uses embedded compliance channel

USB 3.0 Superspeed PHY Test Report

Overall Results: 2 of 14 Tests Failed

Test Configuration Details	
Device Description	
De-embed Settings	Embed
Input Signal Type	Live signal
Reference Clock	SSC
De-emphasis Mode	-3.5 dB
Device	Device
Test Session Details	
Infiniium SW Version	02.10.0004
Infiniium Model Number	DSO91304A
Infiniium Serial Number	No Serial
Application SW Version	1.19.9020
Compliance Limits (official)	USB 3.0 Specification version 1.0
Last Test Date	3/24/2010 10:08:33 AM

Summary of Results

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

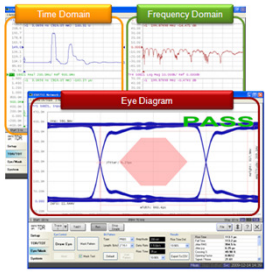
Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✓	0	1	LFPS Peak-Peak Differential Output Voltage	1.1022V	24.5 %	800.0mV <= VALUE <= 1.2000V
✓	0	1	LFPS Period (tPeriod)	51.1841ns	39.0 %	20.0000ns <= VALUE <= 100.0000ns
✓	0	1	LFPS Burst Width (tBurst)	1.2348µs	20.7 %	600.0ns <= VALUE <= 1.4000µs
✓	0	1	LFPS Repeat Time Interval (tRepeat)	10.2417µs	47.0 %	6.0000µs <= VALUE <= 14.0000µs
✓	0	1	LFPS Rise Time	136.3ps	96.6 %	VALUE <= 4.0000ns
✓	0	1	LFPS Fall Time	140.6ps	96.5 %	VALUE <= 4.0000ns
✓	0	1	LFPS Duty cycle	49.9876%	49.9 %	40.0000% <= VALUE <= 60.0000%
✗	1	1	Unit Interval (with SSC)	201.068ps	-0.7 %	199.940ps <= VALUE <= 201.060ps
✗	1	1	SSC Deviation	5.339964kppm	-2.5 %	3.700000kppm <= VALUE <= 5.300000kppm
✓	0	1	Far End Random Jitter	170mUI	26.1 %	VALUE <= 230mUI
✓	0	1	Far End Maximum Deterministic Jitter	302mUI	29.8 %	VALUE <= 430mUI
✓	0	1	Far End Total Jitter at BER-12	472mUI	28.5 %	VALUE <= 660mUI
✓	0	1	Far End Template Test	0.000	100.0 %	VALUE = 0.000
✓	0	1	Far End Peak-Peak Differential Output Voltage	926.9mV	24.8 %	100.0mV <= VALUE <= 1.2000V

SSC failures are a challenge

USB 3.0 Cable/Connector Compliance Test Solution

ENA Option TDR Solution Configuration

- ENA Mainframe
  - E5071C-480: 4-port, 9kHz to 8.5GHz
  - E5071C-485: 4-port, 100kHz to 8.5GHz
  - E5071C-4D5: 4-port, 300kHz to 14GHz
  - E5071C-4K5: 4-port, 300kHz 20GHz



- Enhanced Time Domain Analysis Option (Option TDR)

- Calibration Standard (Time Domain)
  - ECal Module
    - N4431B for E5071C-480/485
    - N4433A for E5071C-4D5/4K5

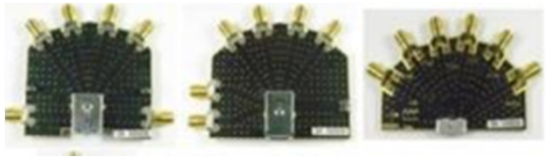
or

  - Mechanical Calibration Kit
    - 85033E-100 for E5071C-480/485
    - 85052D for E5071C-4D5/4K5

Cable Test Fixtures

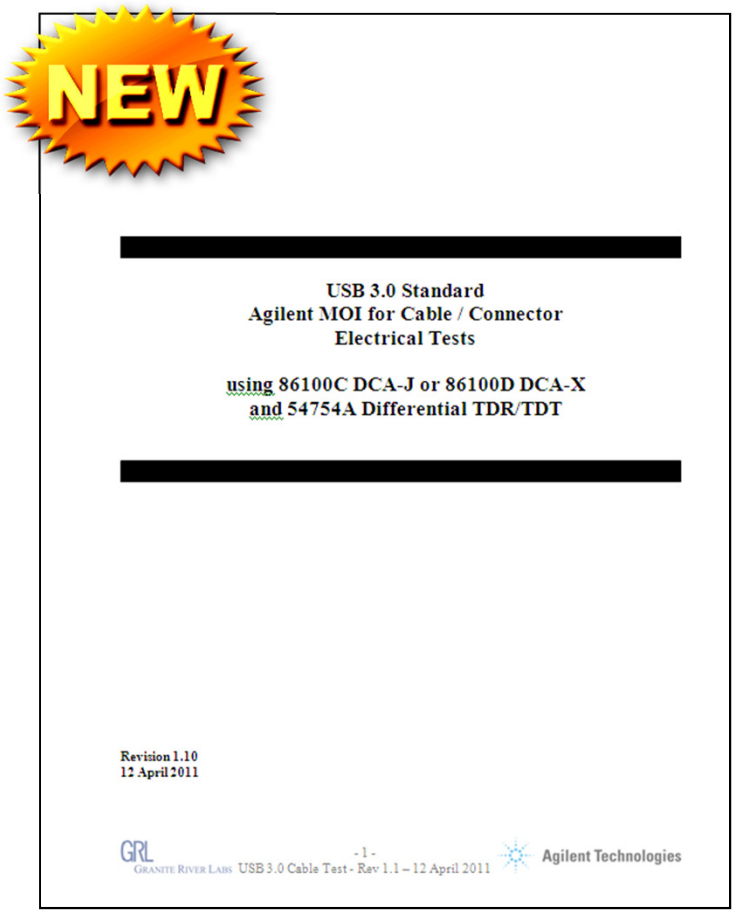
Official Fixtures for testing cable assemblies and connectors are required. Below is a set of fixtures for USB 3.0 cable assemblies and connectors.

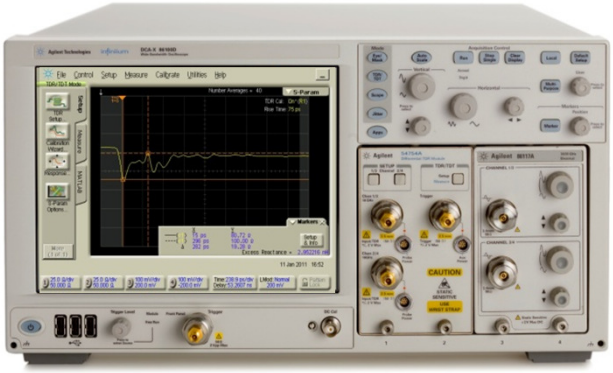
Available for purchase through Allion and BitifEye.
http://www.usb.org/developers/ssusb/ssusbtools/



USB 3.0 Cable-Connector Compliance Test MOI

using Agilent 86100C/D DCA Mainframe and 54754A TDR/TDT Module





USB 3.0 Spec Reference	Test Description	Cable 1		Cable 2		Cable 3		Cable 4		Cable 5		Cable 6	
		DCA-TDR	ENA-TDR	DCA-TDR	ENA-TDR	DCA-TDR	ENA-TDR	DCA-TDR	ENA-TDR	DCA-TDR	ENA-TDR	DCA-TDR	ENA-TDR
5.6.1.2	Mated Conn Diff Impedance												
	X cable end, TX pair	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL	PASS	PASS	PASS	PASS
	X cable end, RX pair	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS	FAIL	PASS	PASS	PASS	PASS
	Y cable end, TX pair	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	Y cable end, RX pair	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
5.6.1.3.4	Diff to Common Conversion												
	TX pair, X end to Y end	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL
	TX pair, Y end to X end	PASS	PASS	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL
5.6.1.3.3	DD NEXT, Y end, TX to RX	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
	DD NEXT, X end, RX to TX	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	DD FEXT, X D to Y TX	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	DD NEXT, Y end, D to TX	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	DD NEXT, Y end, D to RX	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	DD FEXT, Y D to X TX	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	DD FEXT, Y D to X RX	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS

Excellent correlation between Agilent DCA-TDR and ENA-TDR based methods

In recent testing at USB3.0 Workshop in April 2011:

- 107 of 108 tests had the same Pass/Fail results
- only 1/108 tests reported Pass (DCA) vs Fail (ENA); the device "straddled" the spec line.

- **Step-by-Step Method of Implementation (MOI)** developed by Granite River Labs (GRL) in cooperation with Agilent Technologies.

Agilent Technologies

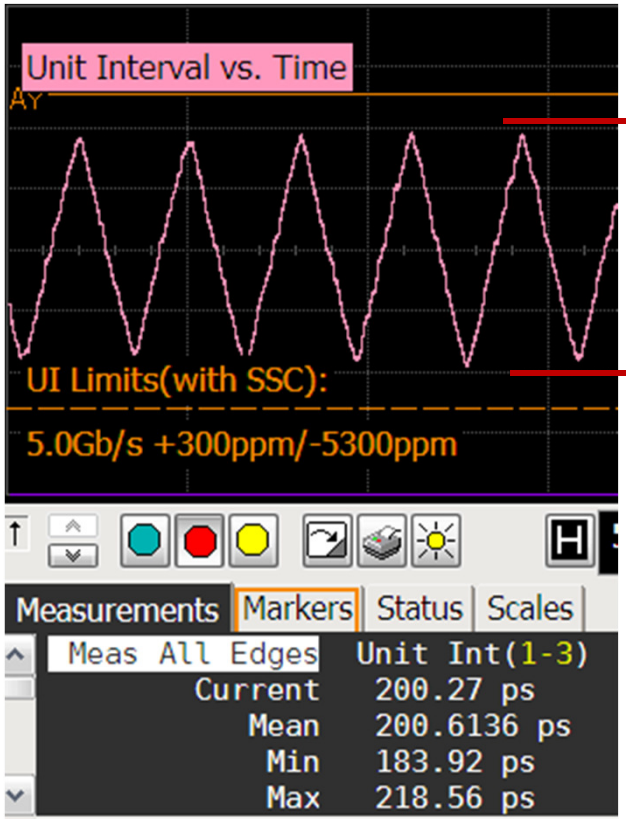
GRL Granite River Labs

USB 3.0 Cable/Connector Compliance Testing is ready: Certification Test Centers Worldwide

ENA option TDR is used by all USB-IF certified test centers to perform USB 3.0 connectors and cable assemblies compliance tests

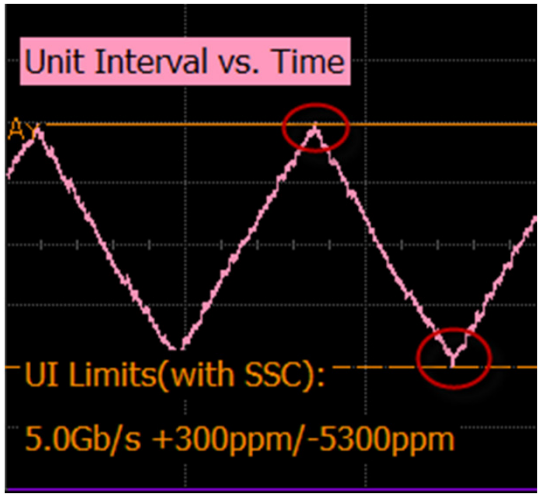
SSC is one of biggest challenges for USB 3.0

- Spread spectrum clocking is the intentional down-spreading of the transmitter's output data rate.

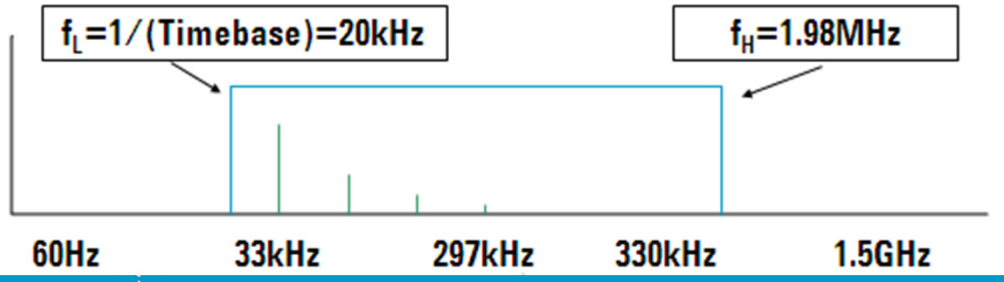


-300ppm

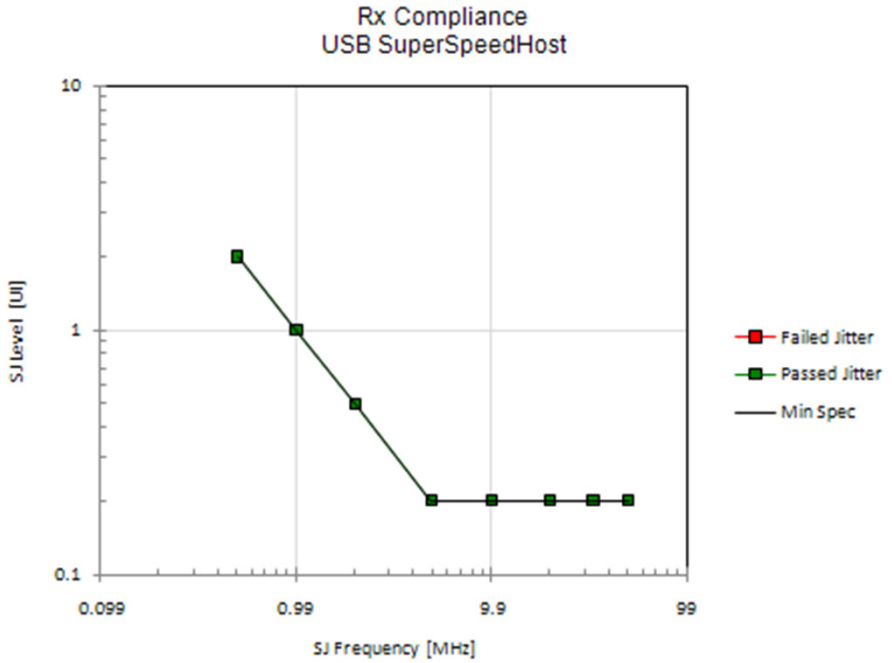
-3700ppm

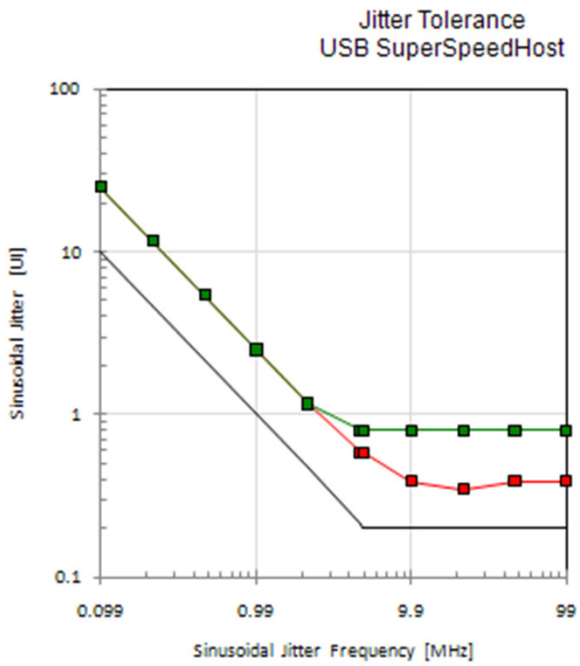


We isolate the 30-33kHz SSC modulation frequency and its relevant harmonics



SuperSpeed Receiver Tests
Rx Compliance and Jitter Tolerance Testing





Result	SJ Frequency [MHz]	Failed Jitter [UI]	Passed Jitter [UI]	Min Spec [UI]	Symbol Errors
pass	0.500		2.00	2.000	0
pass	1.000		1.00	1.000	0
pass	2.000		0.50	0.500	0
pass	4.900		0.20	0.200	0
pass	10.000		0.20	0.200	0
pass	20.000		0.20	0.200	0
pass	33.000		0.20	0.200	0
pass	50.000		0.20	0.200	0

Receiver Test Procedure

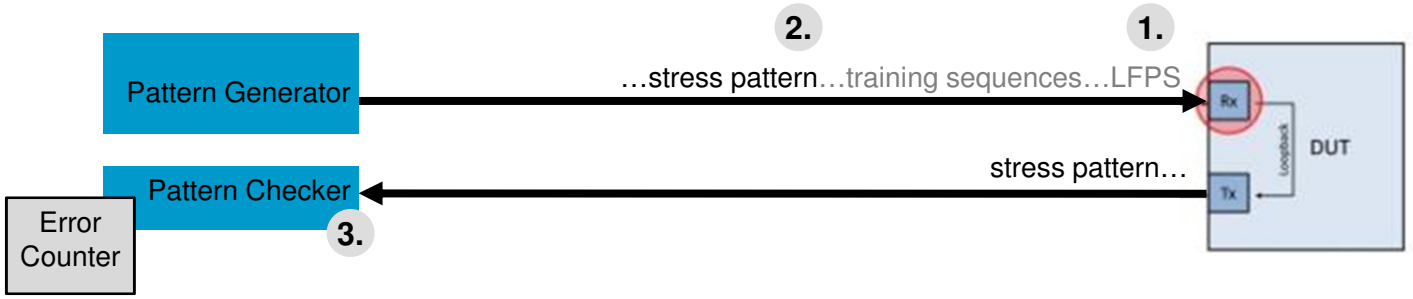
External Error Counter

Turn on loopback by sending LFPS and required training sequences

The receiver stress pattern is BDAT with SKPs inserted as described in the standard.
The pattern checker receives the looped stress pattern BDAT and recognizes bit errors

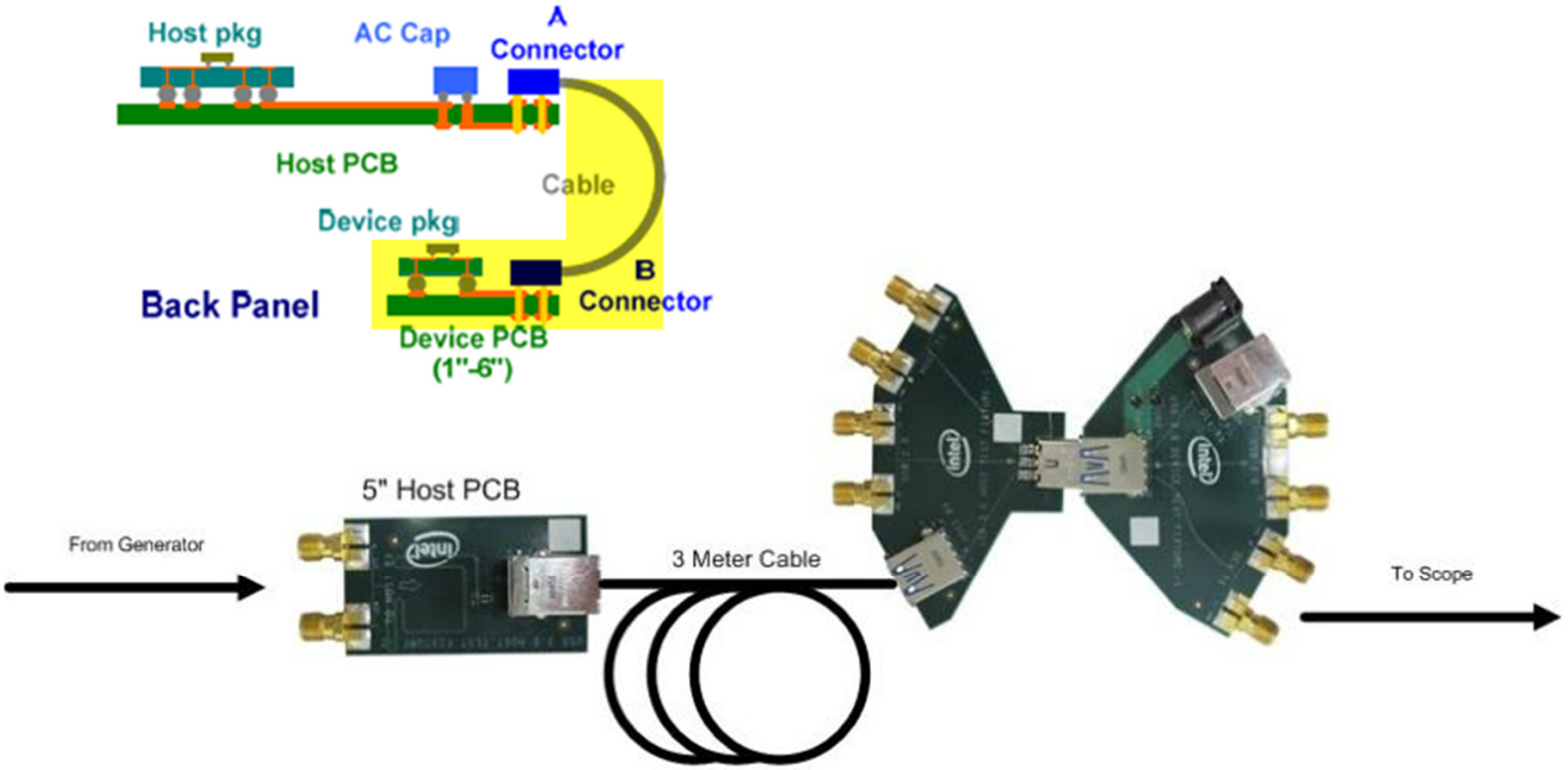
After sufficient test time the error counter of the pattern checker is read

Pattern Generator: J-BERT, ParBERT



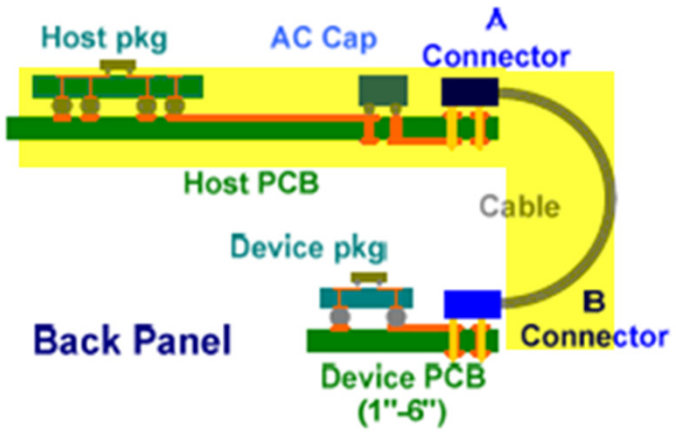
Pattern Checker: JBERTB SER

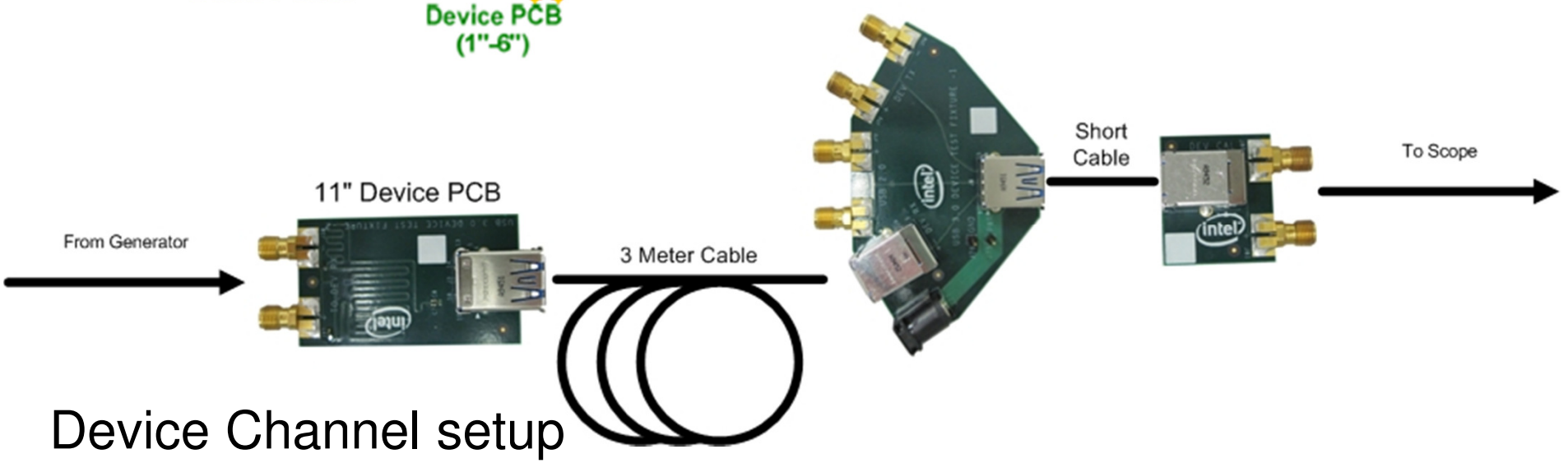
SuperSpeed Host Receiver Test Calibration and compliance channel



Host Channel setup

SuperSpeed Device Receiver Test Calibration and compliance channel

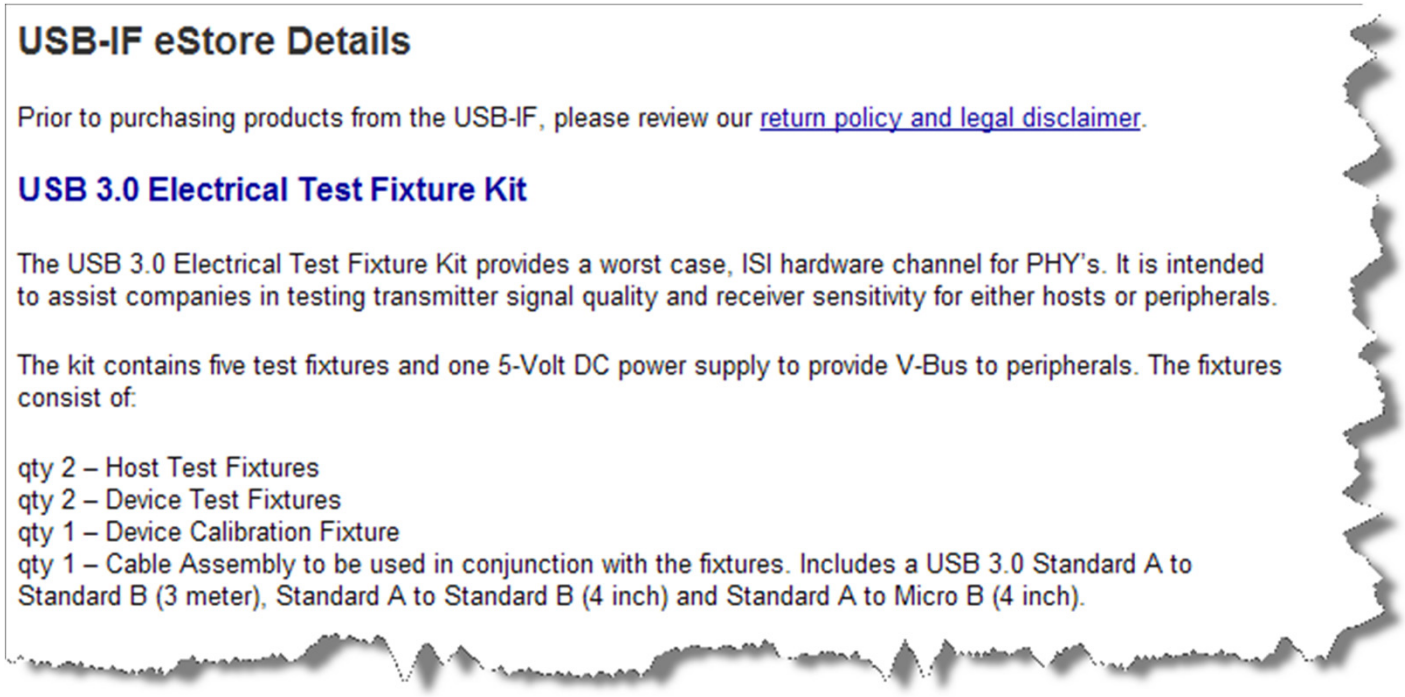




Device Channel setup

Fixtures and cables available from the USBIF at:

http://www.usb.org/developers/estoreinfo/



USB-IF eStore Details

Prior to purchasing products from the USB-IF, please review our return policy and legal disclaimer.

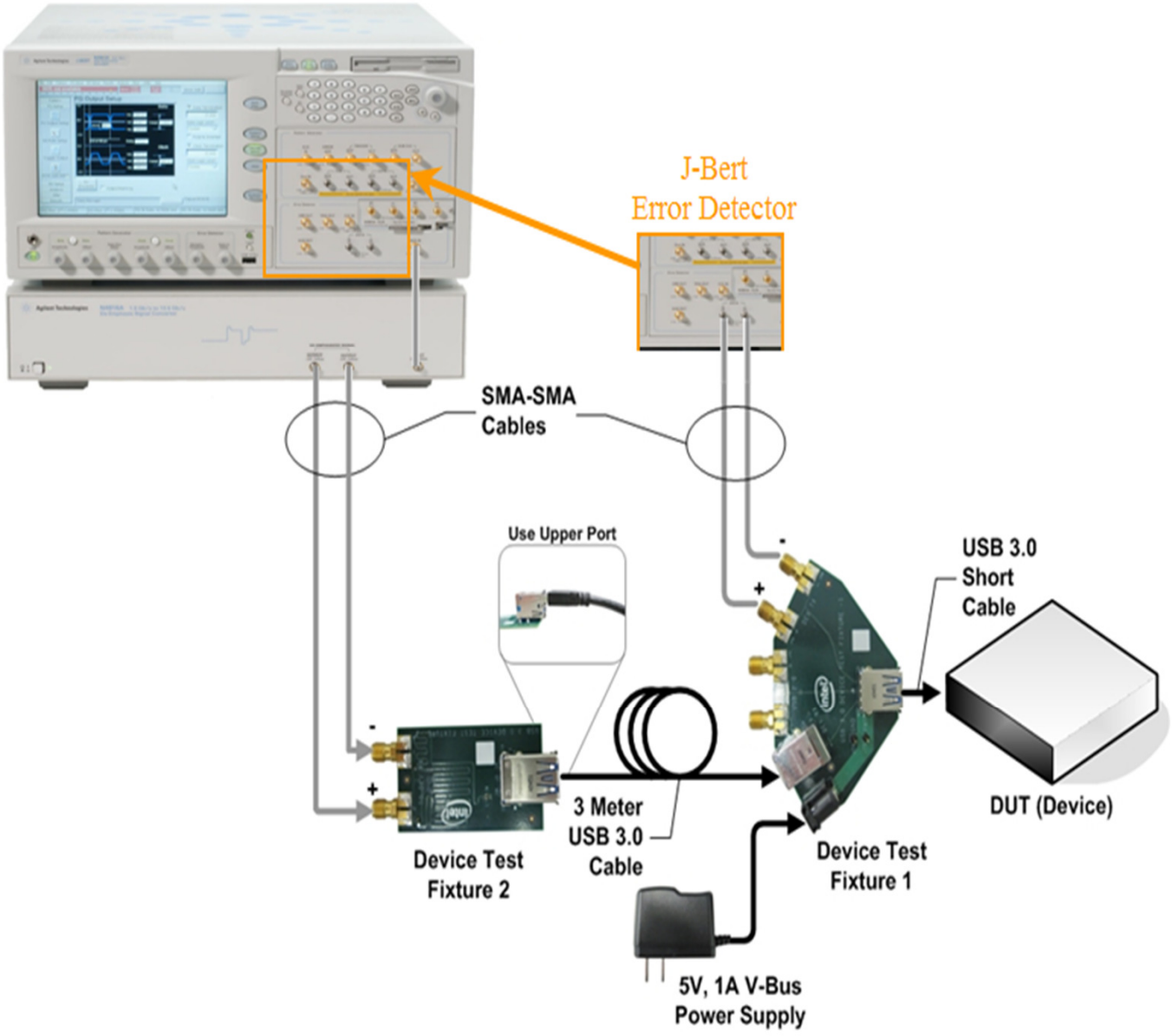
USB 3.0 Electrical Test Fixture Kit

The USB 3.0 Electrical Test Fixture Kit provides a worst case, ISI hardware channel for PHY's. It is intended to assist companies in testing transmitter signal quality and receiver sensitivity for either hosts or peripherals.

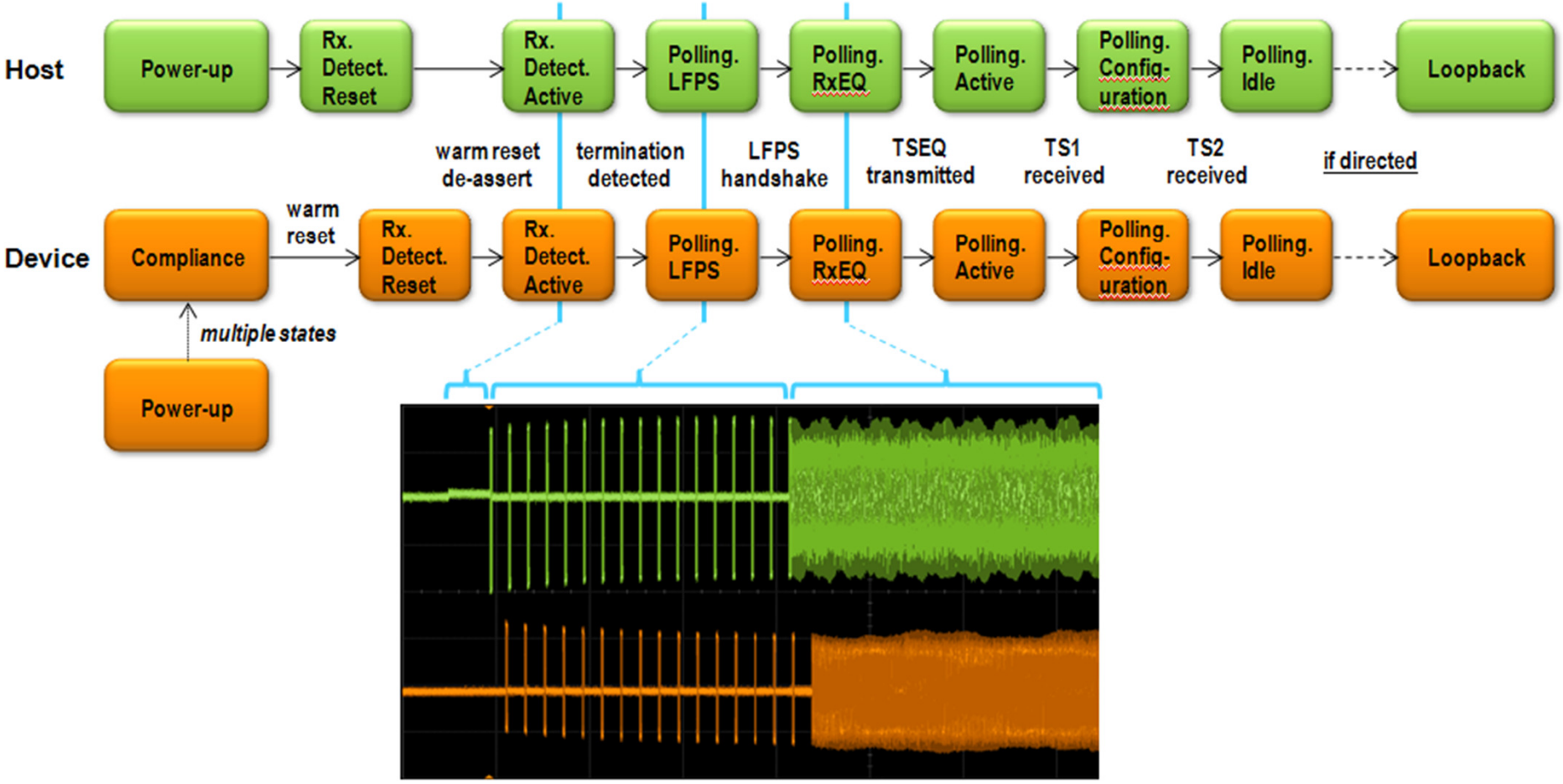
The kit contains five test fixtures and one 5-Volt DC power supply to provide V-Bus to peripherals. The fixtures consist of:

qty 2 – Host Test Fixtures
qty 2 – Device Test Fixtures
qty 1 – Device Calibration Fixture
qty 1 – Cable Assembly to be used in conjunction with the fixtures. Includes a USB 3.0 Standard A to Standard B (3 meter), Standard A to Standard B (4 inch) and Standard A to Micro B (4 inch).

SuperSpeed Receiver Test Calibration and compliance channels



Typical SuperSpeed Link Turn-on Sequence



Standard Loopback Entry Sequence

- Power on the device under test.
- Transmit 200 Polling.LFPS (2ms).
  - Note that all jitter sources are added during all transmissions to the device under test. If the device does not go into loopback it fails the test.
- Transmit 65536 TSEQ.
- Transmit 256 TS1.
- Transmit 256 TS2 with loopback bit set.
- Start transmitting the BDAT test pattern.
- Transmit BDAT for 2 ms before starting error calculations.
- Transmit the BDAT sequence from the signal source for a total of 3x109 symbols (3x1010 bits). A single SKP ordered set is inserted in the sequence every 354 symbols.

➢ If a DUT under test does not enter loopback with this sequence it is technically a failure.

Host and Hub Drop/Droop testing

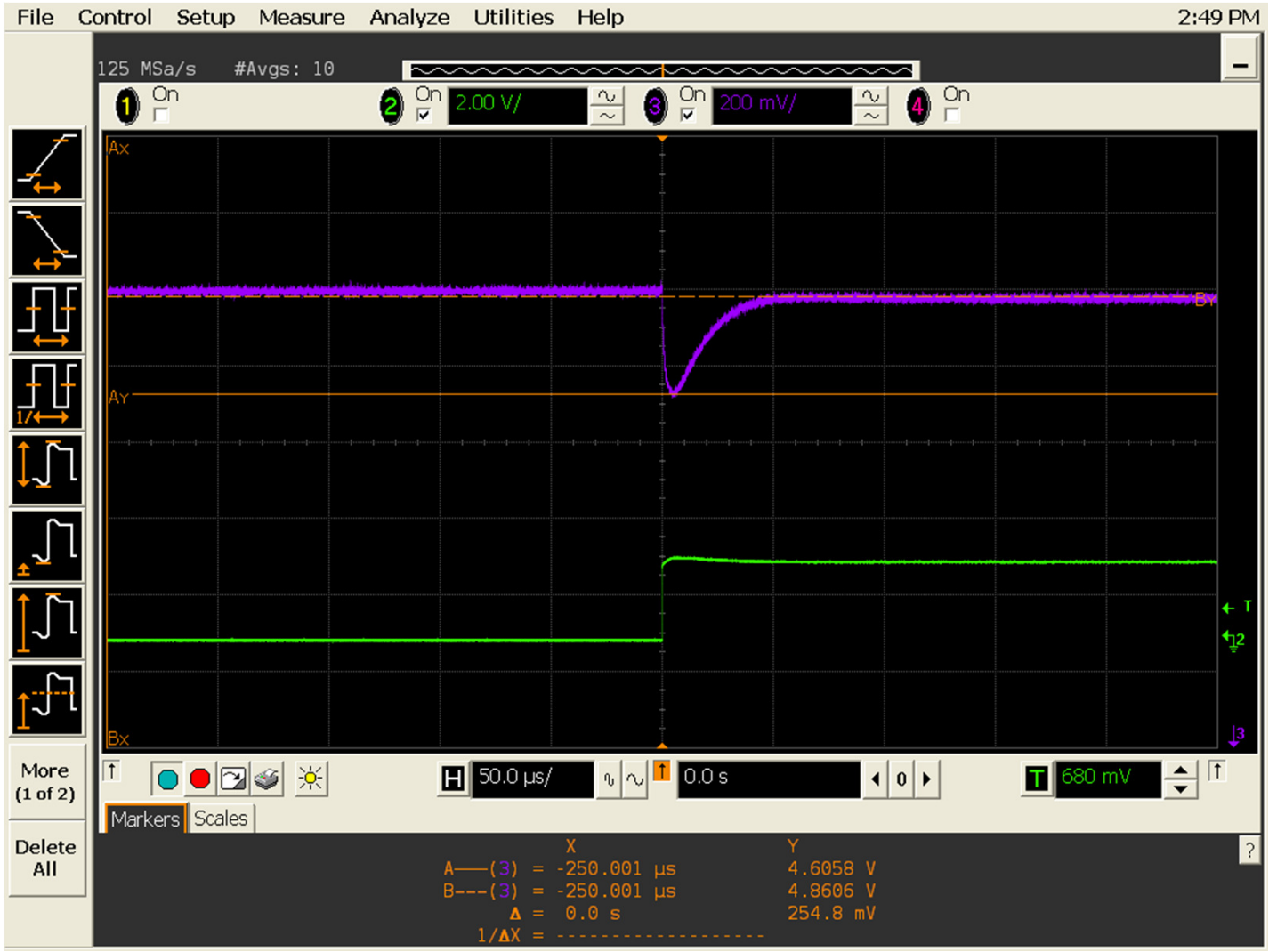
- Un-configured power is now 150mA
- High power devices can draw up to 900mA
- A new Drop-Droop fixture is available from the USB-IF
- Drop test verifies fully that a host or hub maintains Vbus levels within spec under full load conditions
- Droop Test verifies inrush event on adjacent port will not cause Vbus to “droop” beyond specification.

USB 3.0 Drop-Droop Fixtures

The USB 3.0 Drop Droop fixtures assist companies in testing voltage drop and droop levels for hosts or hubs.

The fixture is shipped as a standalone fixture. Vendors are responsible for the 4" cables required to be used in conjunction with the fixture. The cost of the fixture is US$275 (members) and US$325 (non-members). The software to use with the fixture is available for download on the USB Tools page. **Please direct questions regarding the fixtures to ssusbcompliance@usb.org.**

Host Droop Test Result



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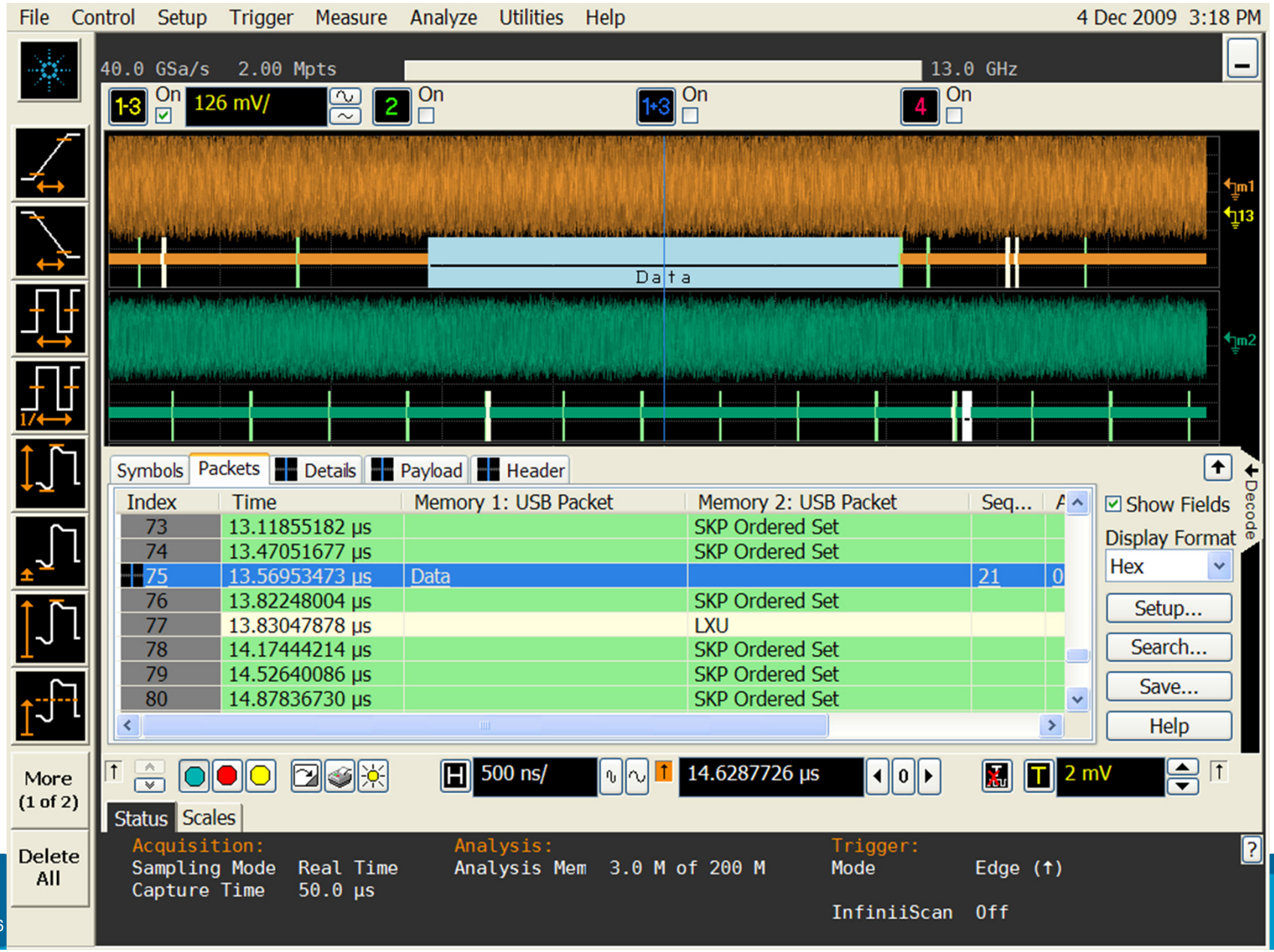
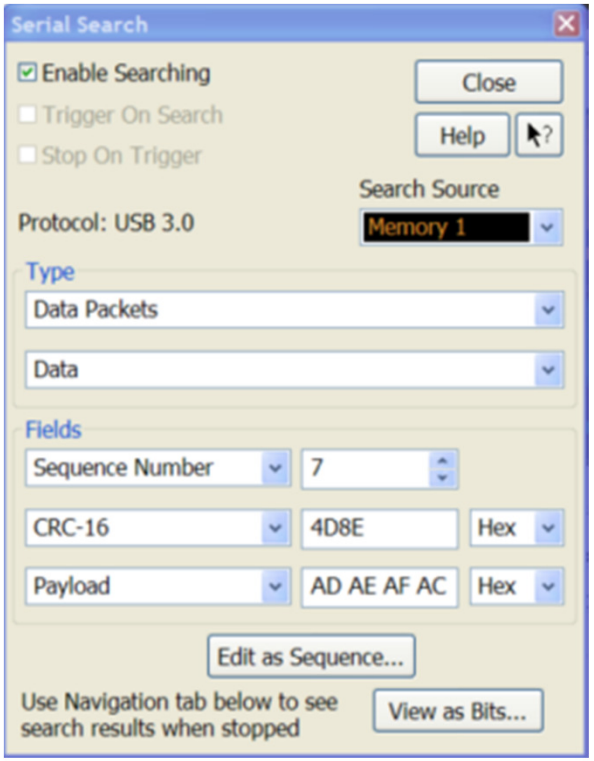
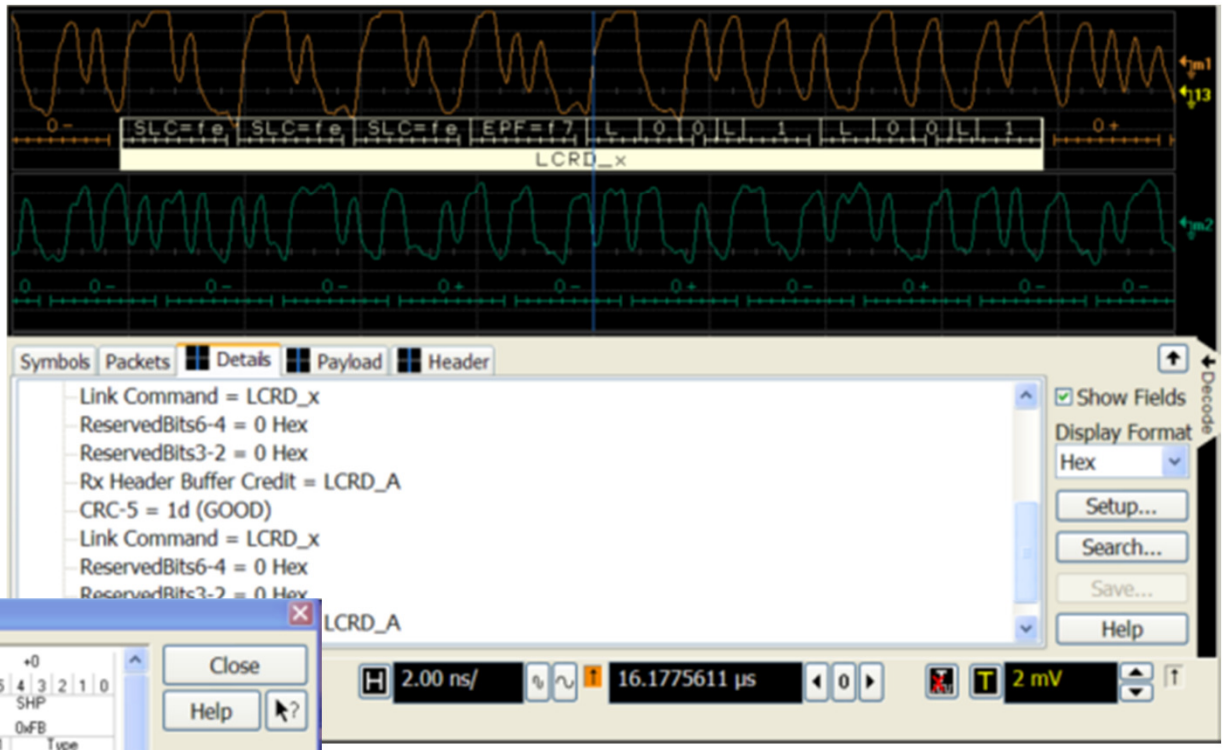
USB 3.0 Protocol Decode: on scope

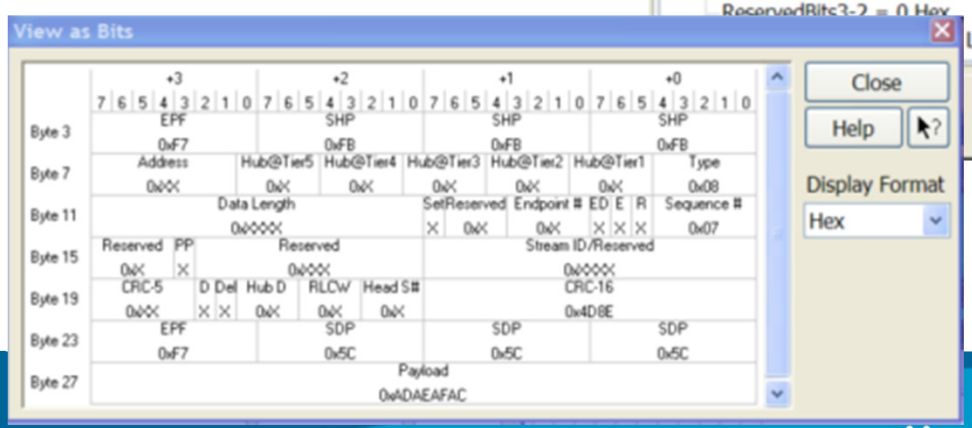


Additional USB 3.0 Protocol Capabilities



- Search and trigger
- Views: Details, Payload, Header





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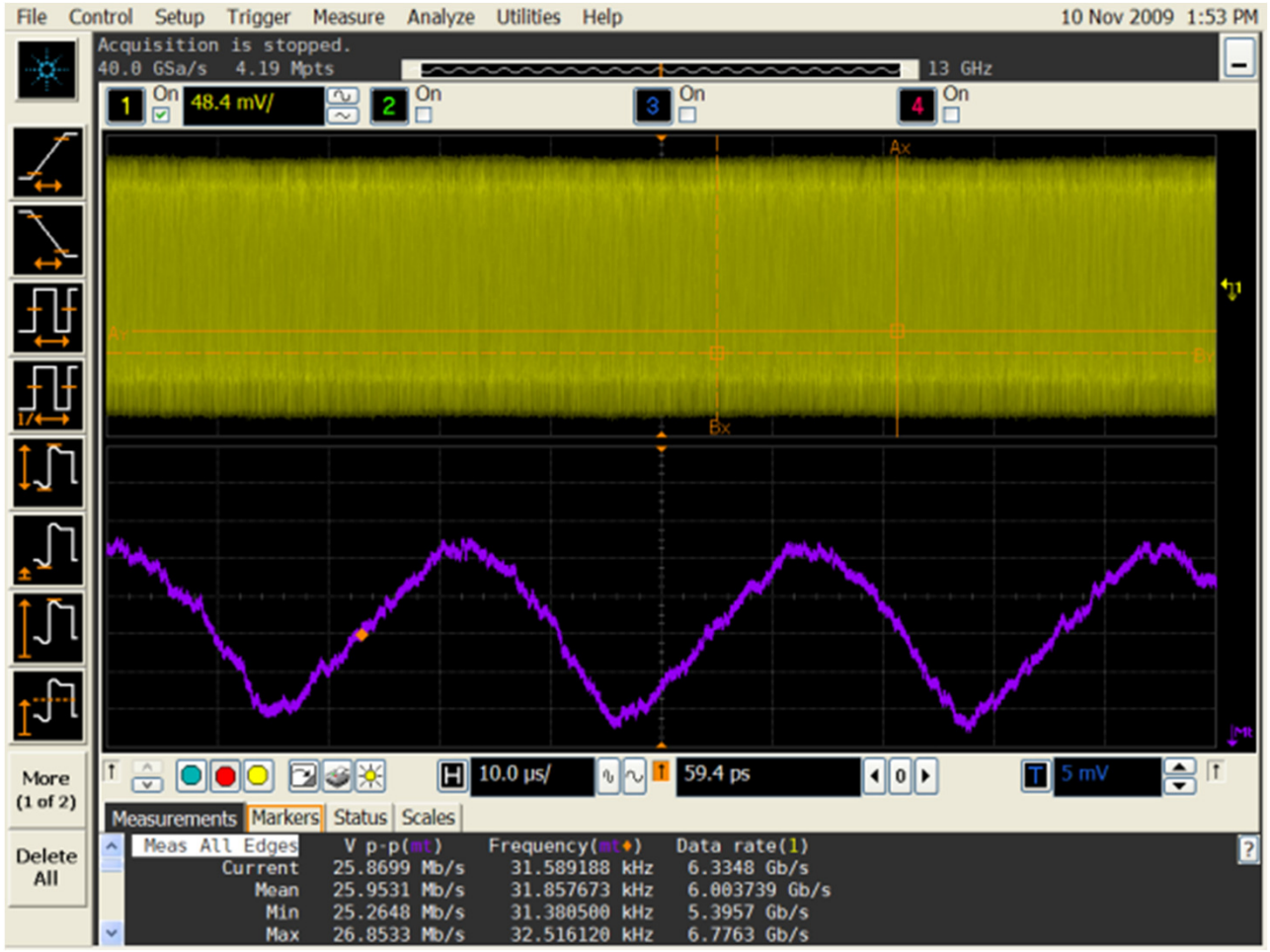
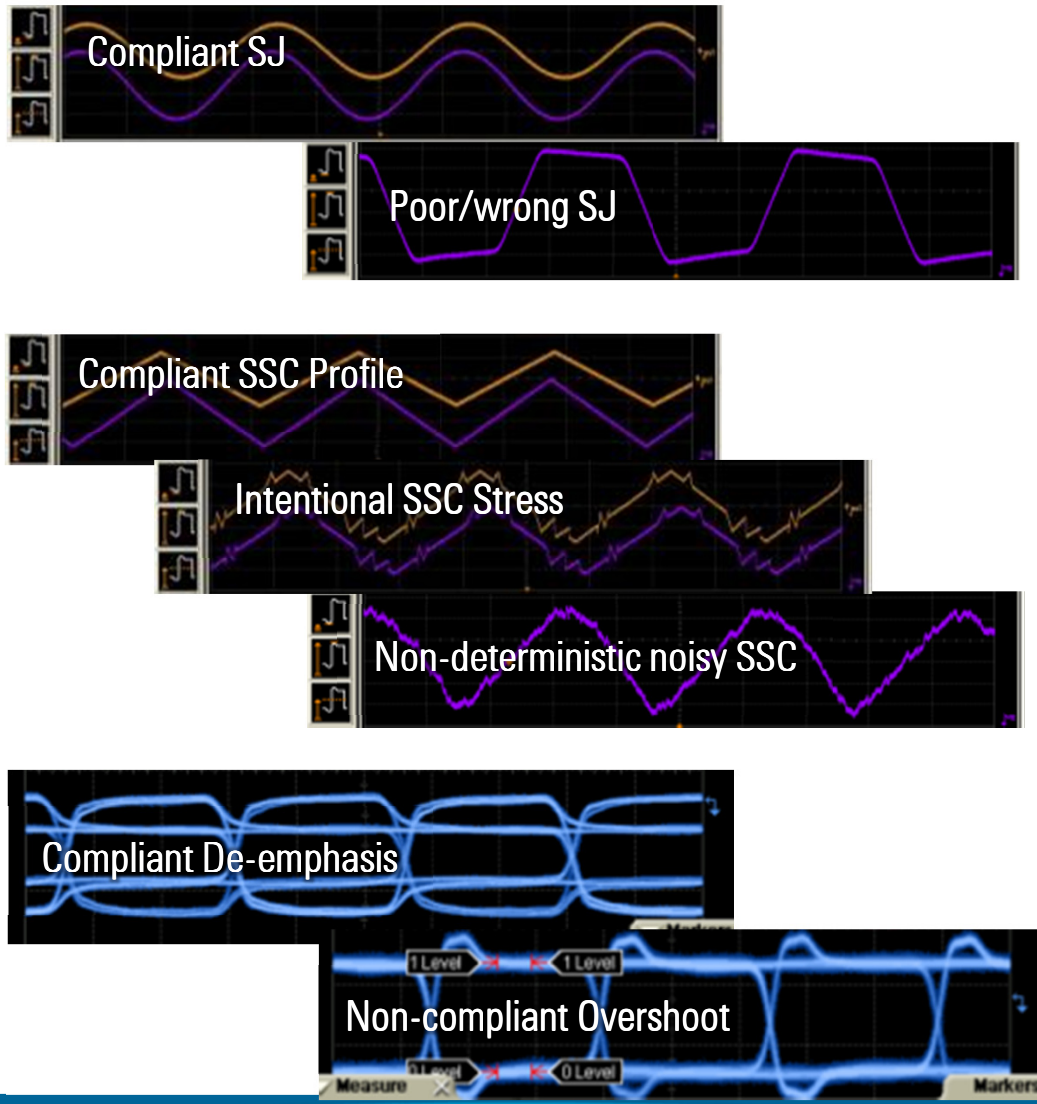
TX Compliance Pitfalls



- SSC modulation
- SSC deviation
- High Rj (flicker Jitter)
- Poor de-emphasis
  - Cause eye failure at end of channel

RX Compliance Pitfalls

- Loopback issues
  - Dut needs custom sequence
  - DUT drops out easily
- Calibration issues
  - Inconsistent
  - Poor Sj/Rj mod
- SSC deviation
- invalid de-emphasis
  - Great impact on TJ



Don’t forget USB 2.0 Compliance Pitfalls

Failure to properly support USB suspend

- Low power state required of all devices
  - < 2.5mA (spec says 500uA = auto waiver)

Improperly report bus vs self powered if battery powered

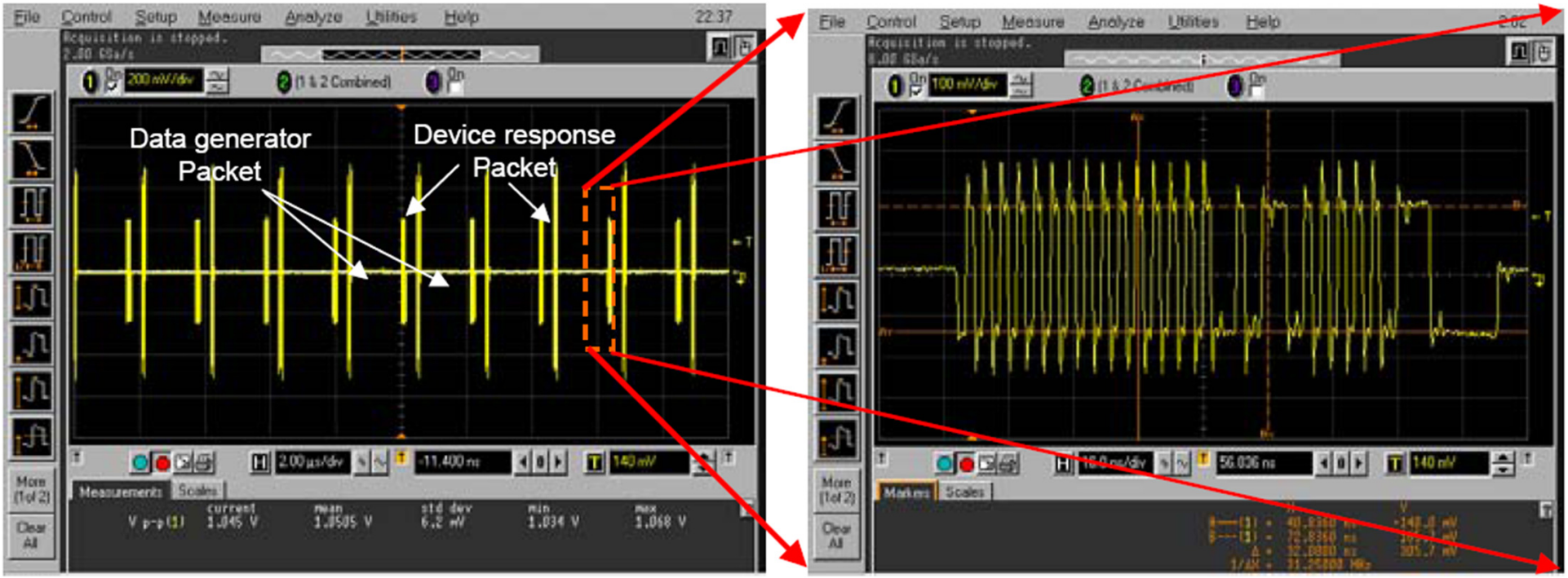
RX Sensitivity failure vs Squelch

Backdrive

SW Driver loading sequence

Test mode not implemented

Compliance Pitfalls – RX Test



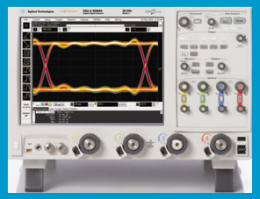
- Misinterpretation of RX sensitivity and Squelch requirements has caused considerable confusion and discrepancy in test results
- As you can see from the waveform at the right the artifacts on the transition and non-transition bits due to reflections are significant

Agilent USB 2.0 and USB 3.0 Total Solution

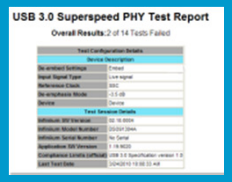
PHYSICAL LAYER

Transmitter Characterization (PHY/TSG/OOB)

DSAX93204A oscilloscope



U7243A USB 3.0 and N5416A USB 2.0

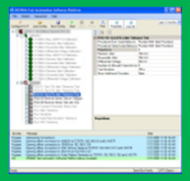


N8805A USB 3.0 Protocol viewer software

Receiver Jitter Tolerance Testing

N4903B High-performance JBERT with SER Counter

N4916B De-emphasis Converter



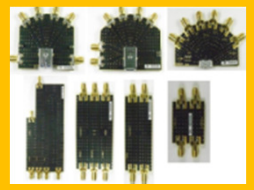
N5990A Automated compliance and device characterization test

Cable/Connector

E5071C Network Analyzer

Option TDR

N4433A Ecal Module



USB 3.0 Cab/conn test fixture kit from BitifEye

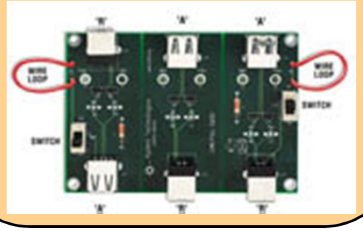
Test Fixtures

USB2 and USB3

U7242A USB 3.0 Fixture

E2649B USB 2.0 Fixtures

E2646A SQiDD



Industry's lowest scope noise floor/sensitivity and trigger jitter

Automated compliance software accurate, efficient, and consistent

Industries fastest and highest accuracy cable and connector test soln

Fixtures for Low Speed, Full Speed High Speed and SuperSpeed USB Physical Layer testing

Intel and AMD announce USB 3.0 Chipsets

Intel Will Add Both USB 3.0 and Thunderbolt To Ivy Bridge

April 15, 2011

http://www.newsfactor.com/news/Intel-Adopts-Thunderbolt--USB-3-0/story.xhtml?story_id=033003DQW73R

AMD announces Fusion chipsets with USB 3.0 support

April 13, 2011

"Advanced Micro Devices said it will support USB 3.0, beginning with its A75 and A70M chipsets".

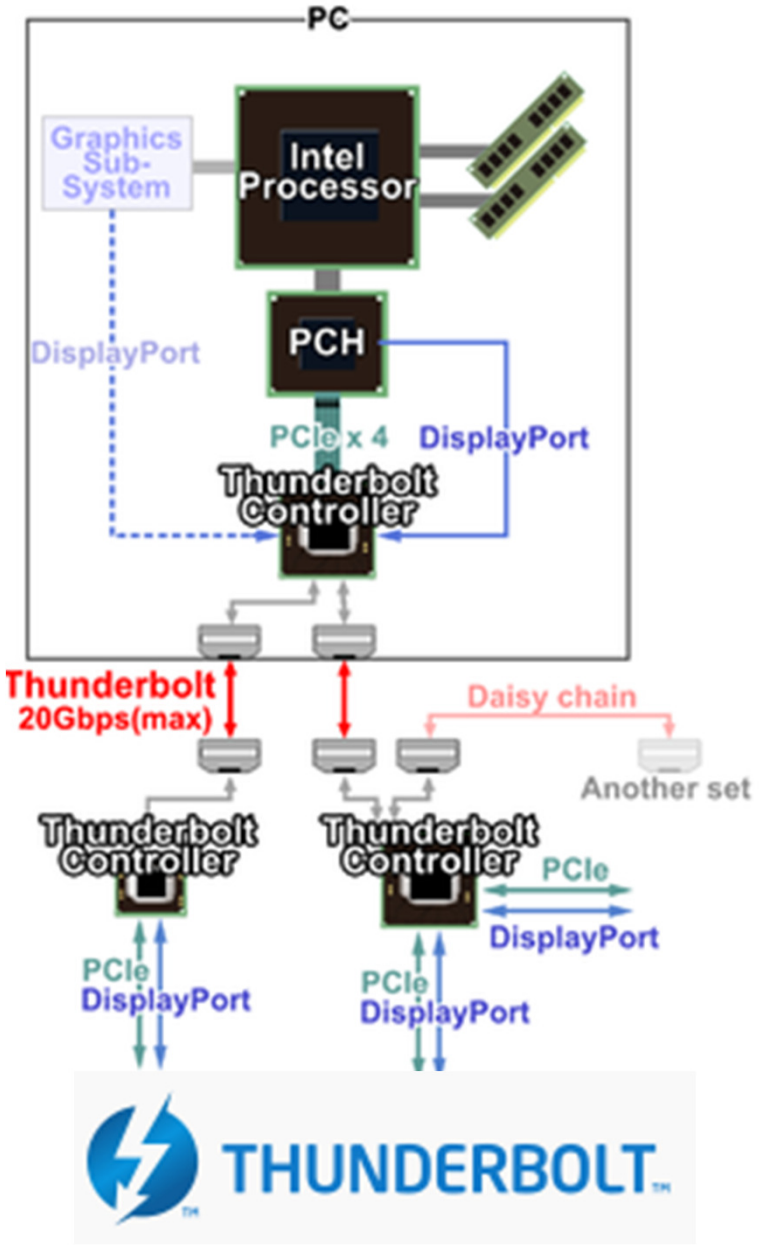
http://www.techspot.com/news/43290-amd-announces-fusion-chipsets-with-usb-30-support.html

What is Thunderbolt?

- *Source: Wikipedia*

http://en.wikipedia.org/wiki/Thunderbolt_(interface)

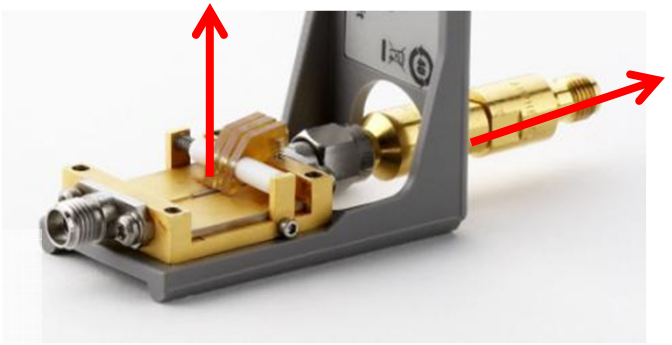
- Connector is Mini DP
- Host side interface x4 PCIe and DP
- External 2x10Gbps TBT links
- Complementary technology with respect to USB 3.0



De-embedding and Precision Probe

- At 5Gbps and above removing probing effects is key
- Typical de-embedding requires accurate s-parameters
- Challenge of using s-parameters is cable variation requires exact measurement for accuracy
- Precision probe + accurate embedding/de-embedding with InfiniiSim will save you significant margin

90000 X-series
CAL output (step)



Save time: Two options for characterization before PrecisionProbe

Option 1: Six steps (you would need to do the following)

Find a VNA

Find a someone that knows how to use a VNA and measure the cable

Create s-parameter file

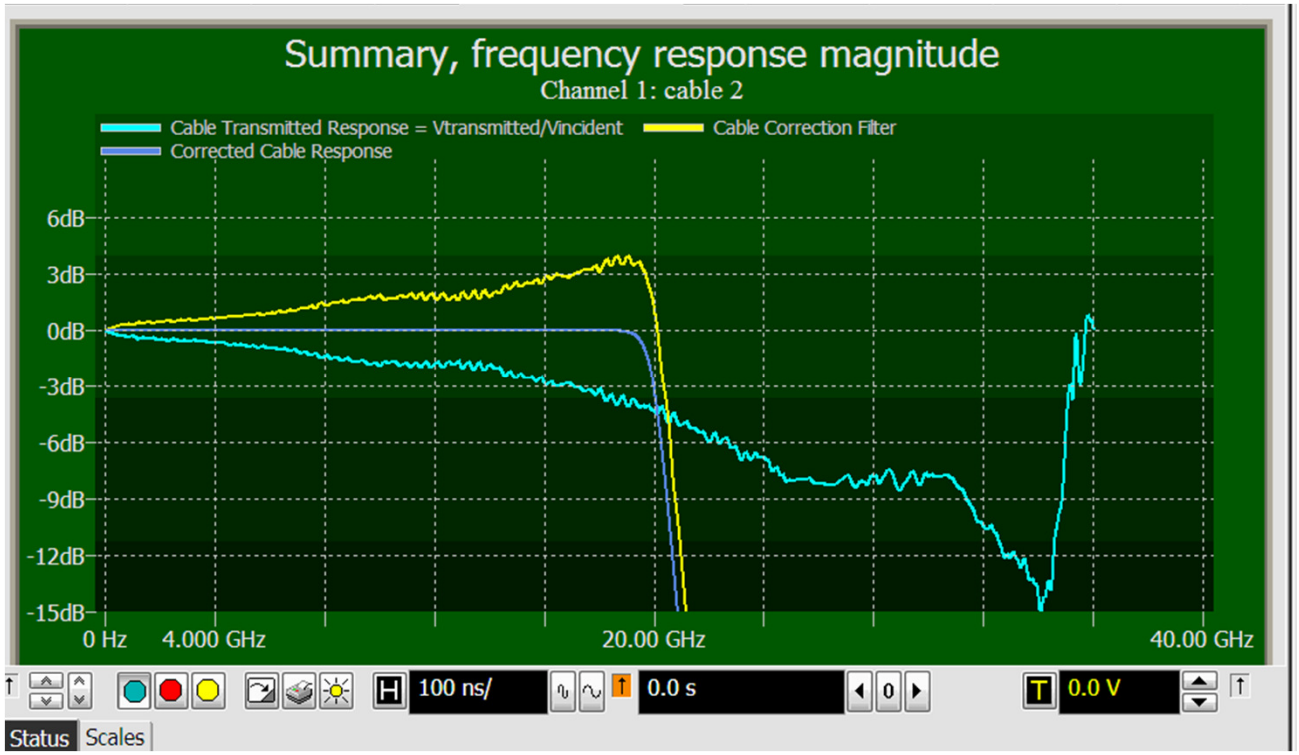
Save s-parameter file to thumdrive and load on scope

Learn waveform transformation software and correctly remove loss

Analyze the data

Option 2: Ignore the cable loss entirely

PrecisionProbe and Cable (N2809A)

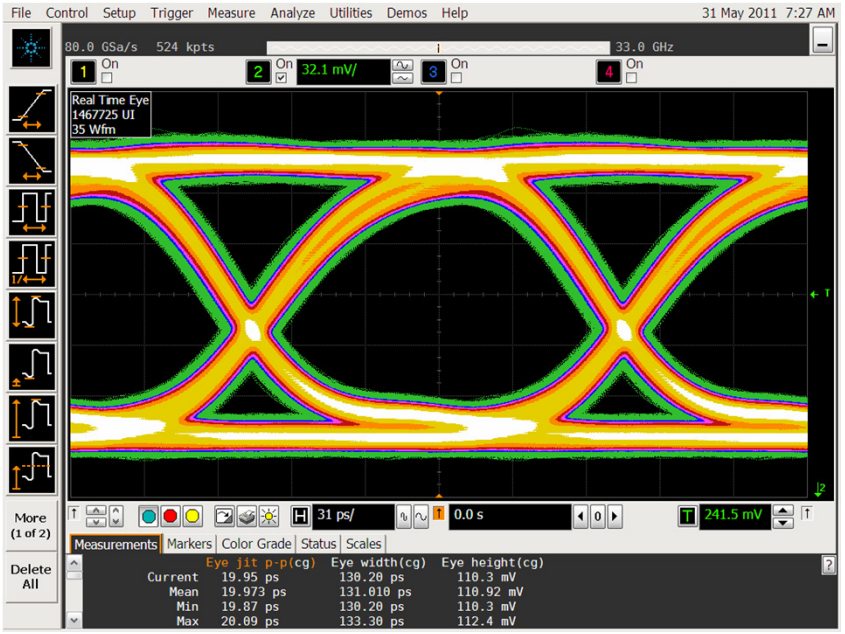


Characterize and correct any input path to your oscilloscope input using only your oscilloscope

The Problem: Measurement Repeatability

Issues that make the problem worse

1. Cables and channels are lossy
2. Probe characteristics are different from probe to probe
3. Switch paths can all vary
4. Custom probes have no oscilloscope correction
5. Tips and probe head correction is typically based off a model and does not represent the exact needed probe
6. Oscilloscope vendors use different frequency response correction methods to account for probing



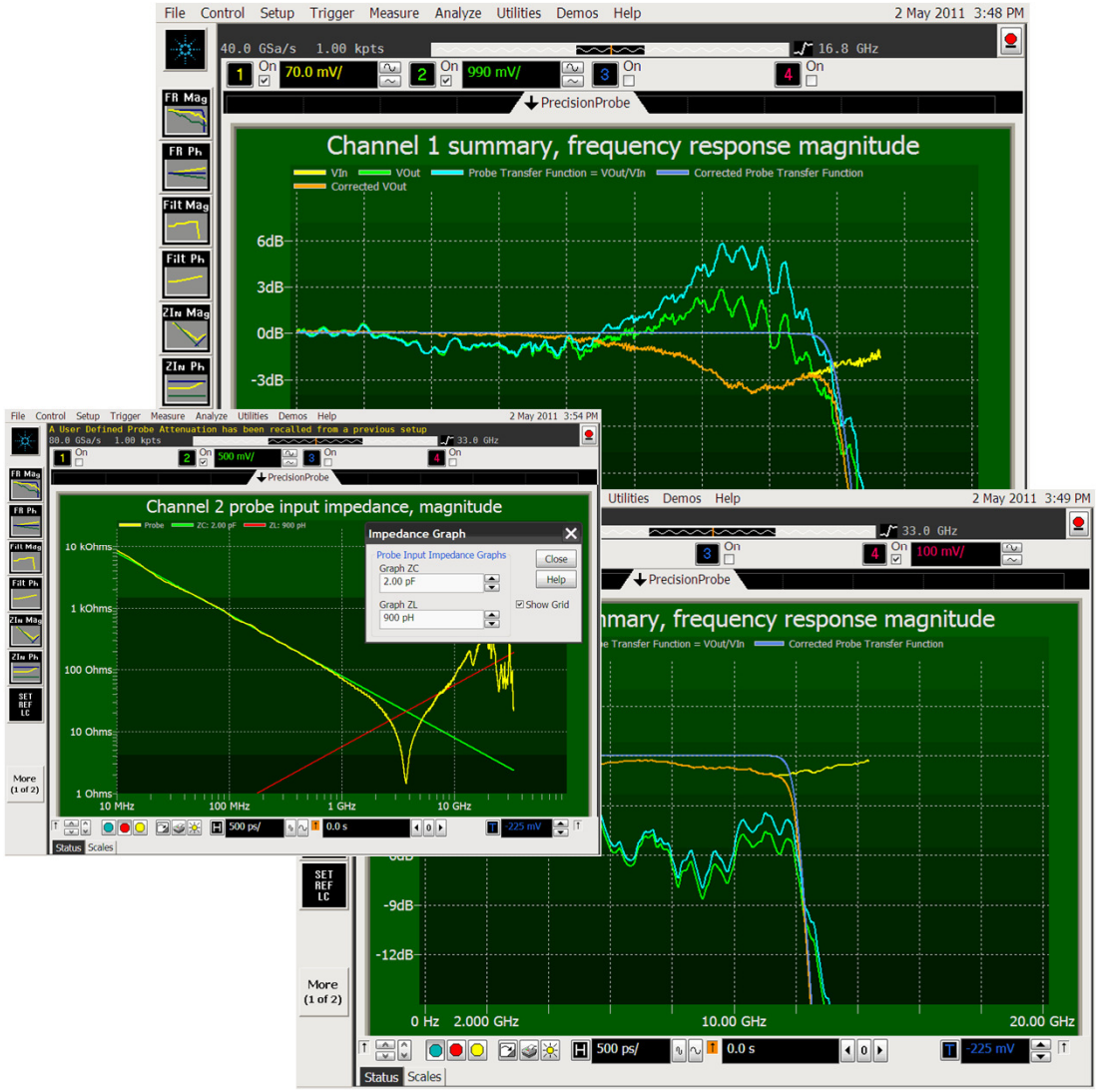
Corrected

Margins are being lost due to connections!

The Solution: PrecisionProbe

PrecisionProbe Quickly and Easily:

- Characterizes and corrects the frequency response (Vout/Vin) of phase of any probe and probe head combination
- Characterizes and corrects for insertion loss caused by cables and fixtures
- Characterizes and corrects for insertion loss caused by switches for probes and cables.



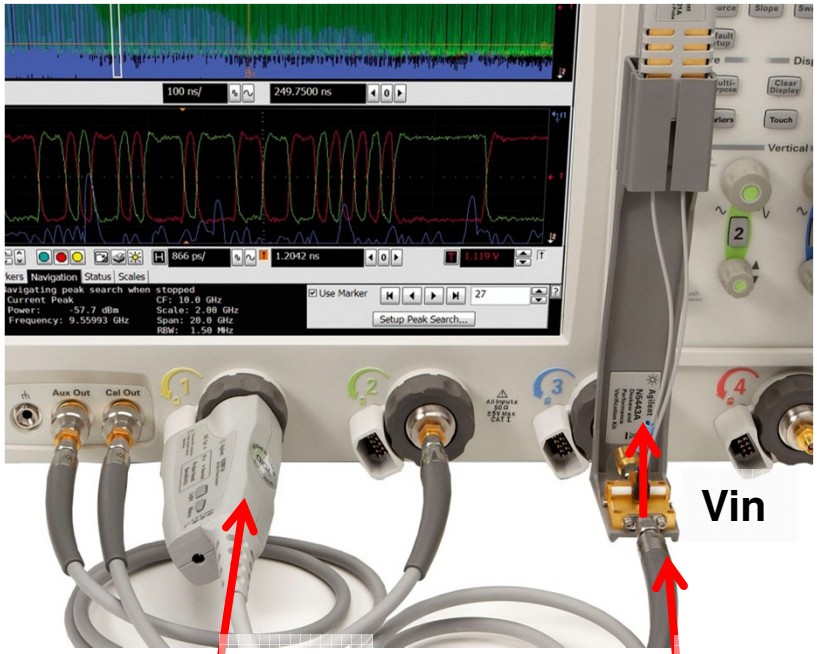
Probes: Key Terms

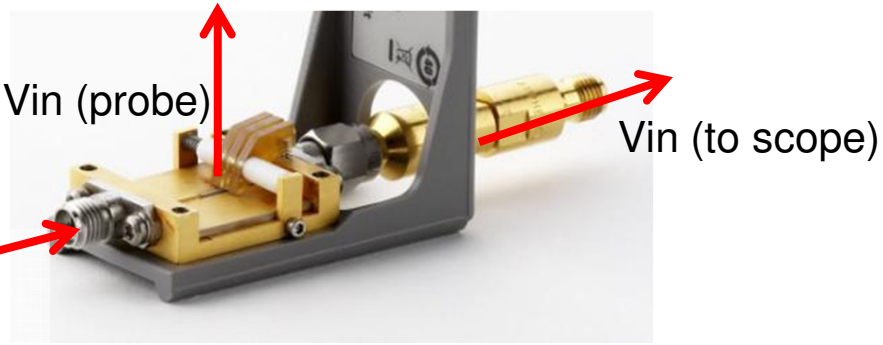
Vin
The signal at the probe point before the probe is connected or the signal at the probe point if an ideal probe were connected

Vsrc
The signal at the probe point as loaded by the probe or the signal at the probe point with the input impedance of the probe loading at that point

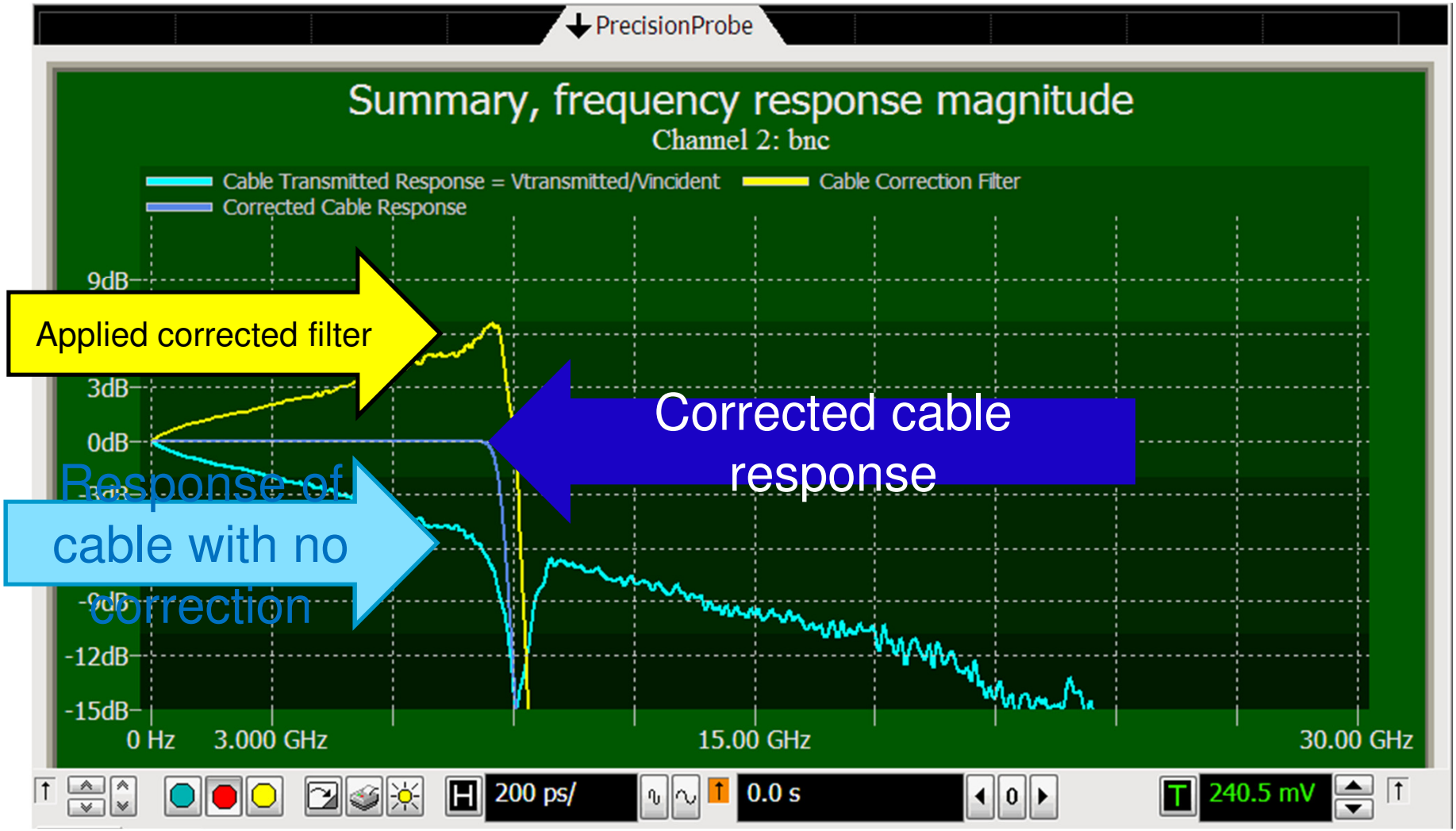
Vout
The signal at the probe point after the probe is connected or the signal at the probe point if a non-ideal probe were connected (reality)

Source impedance
The impedance looking into the probe point. Again: It's the impedance looking into the probe point!

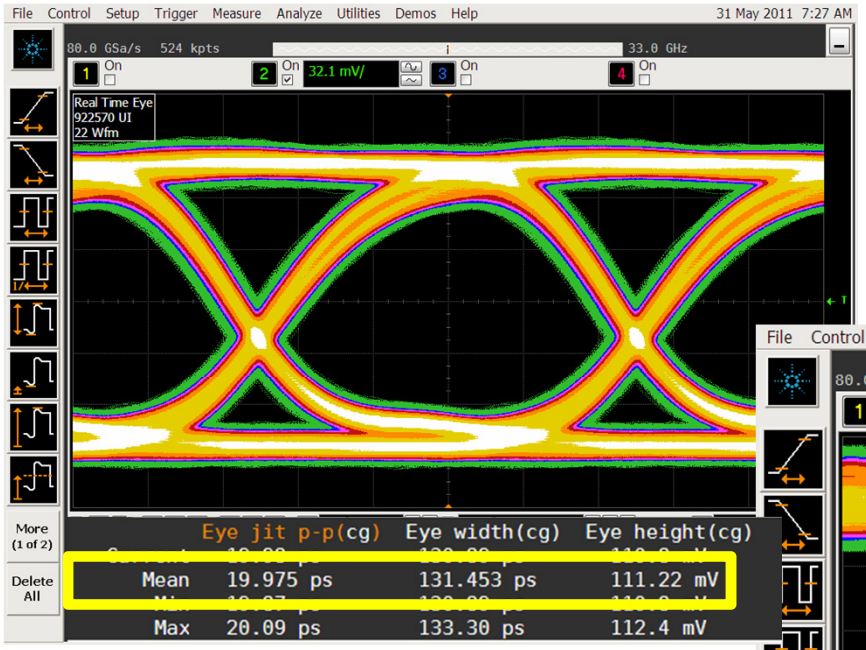


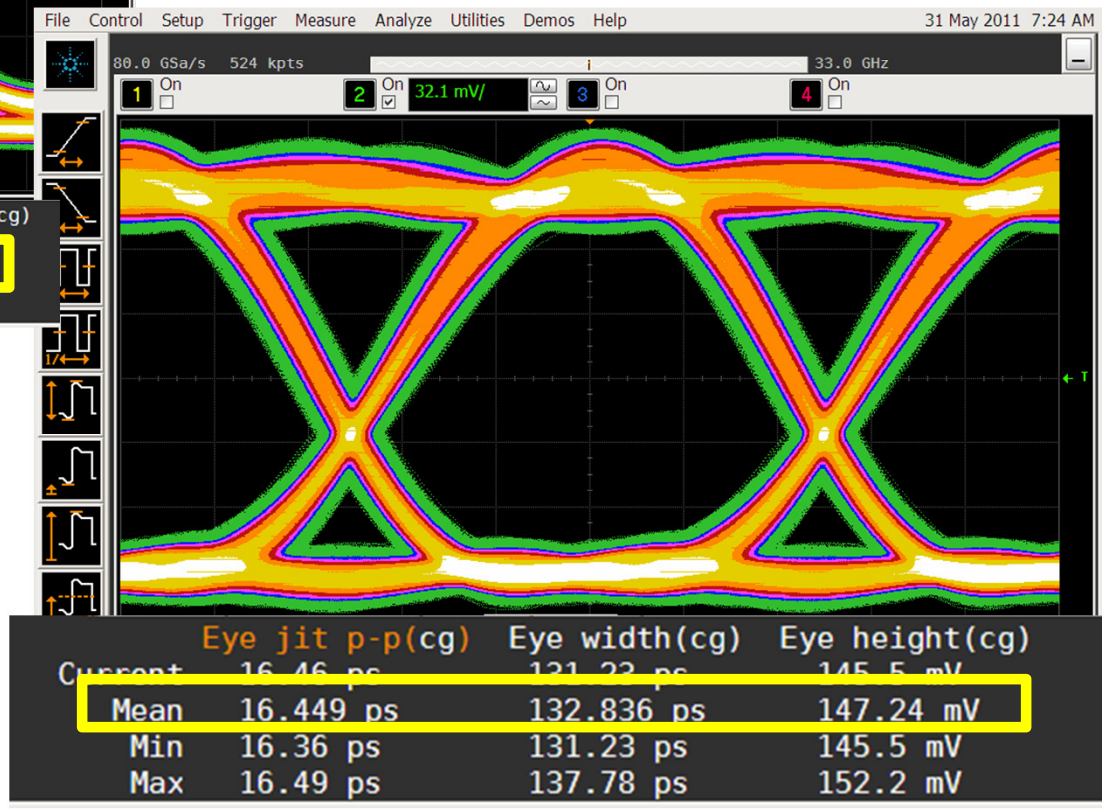


Cables: The result



The real time eye



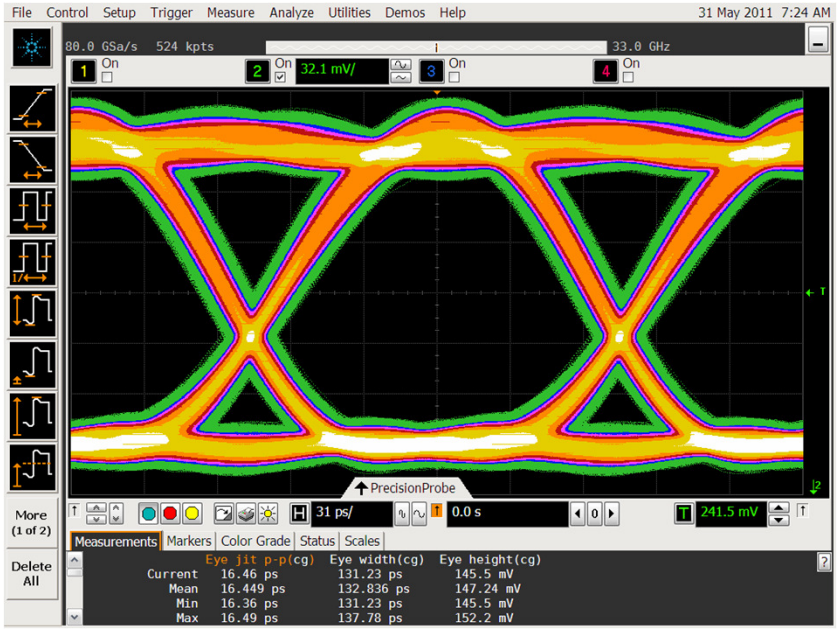


Results: More margins!

20% less jitter
33% more eye height
Slightly wider eye

Summary: PrecisionProbe helps with the following:

1. Cables and channels are lossy
2. Probe characteristics are different from probe to probe
3. Switch paths can all vary
4. Custom probes have no oscilloscope correction
5. Tips and probe head correction is typically based off a model and does not represent the exact needed probe
6. Oscilloscope vendors use different frequency response correction methods to account for probing



By using PrecisionProbe you will further increase your margins without adding significant time or extra equipment

Summary

- USB 3.0 is now in broad adoption phase
- Tools for full TX/RX and channel characterization ready now
- InfiniiSim "compliance channel" emulation without requiring the physical reference channel!
- Agilent's USB 3.0 Compliance solution leverages the ease of use, accuracy and automation delivered by USB 2.0, PCI Express and SATA applications.
- Confidence in our solution comes from our leadership and participation in standards bodies
- Leading solutions adopted by test labs world wide
- Precision Probe to get that last bit of margin back.
- Strong local technical support

- Thanks for attending!

Agilent has the tools and expertise to help you succeed with USB 3.0

Additional references and links

- Agilent Digital Test Solutions:
  http://agilent.eetimes.com/index.html
- USB Implementers Forum, Inc.
  http://www.usb.org/developers
- Agilent N4903B J-BERT:

  http://www.agilent.com/N4903B

  http://www.agilent.com/find/USB
- BitifEye USB 3.0 Cable Test Kit

  http://www.bitifeye.com/cms/front_content.php?idart=213

  www.agilent.com/USB 3.0 Cable Connector Testing MOI

Additional Information

Go to www.usb.org to get additional information on certifying your USB products

For specific updates to compliance requirements go to http://compliance.usb.org/index.html

Agilent Application Note: Debugging USB 2.0: It's Not Just a Digital World

Go to www.agilent.com/find/usb to find more about Agilent Superior Signal Integrity Solutions and Probing for Your Applications