Integration and Certification Challenges for SuperSpeed Host, Hub and Device Solutions

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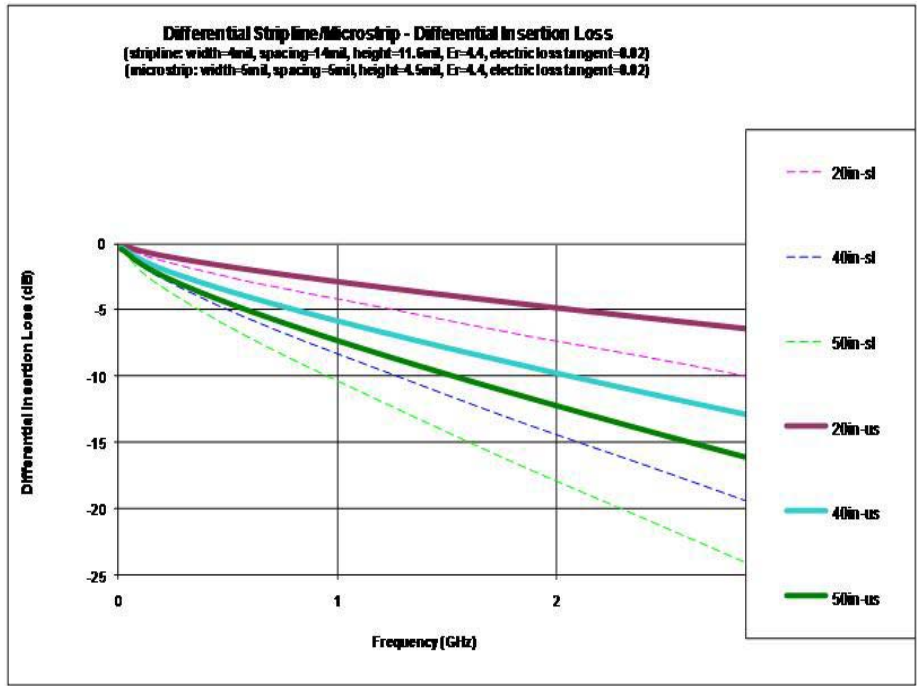
Agenda

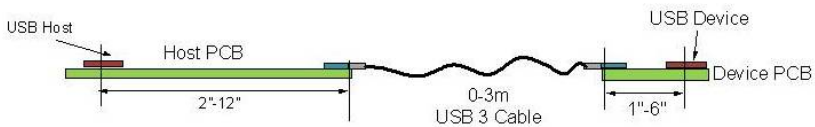
- Differential Pair Routing
- Calibration Resistor
- Power Considerations
- Power Sequencing
- VBUS
- Clocks
- ESD

- TI Product Portfolio
  - SN65LVPE502CP
  - TUSB1310A
    - PIPE
    - ULPI
    - FPGA Timing
  - TUSB9261
  - TUSB8040
  - TUSB7320/7340
- Support & Contacts

Multi-Gbps Differential Pairs

- Attention to signal Integrity is Imperative!
  - Loss profile for various differential trace types over frequency as measured at TI.
  - Example of a 20-inch microstrip
    - at USB 2.0 the insertion loss is about –2 dB
    - at USB 3.0 speed, this approaches –6dB
    - Stripline trace is even worse!
    - In practical designs, the trace used to connect from a USB 3.0 device to the connector is a combination of microstrip and stripline.
- Trace, cable and connectors lead to dispersion of single-bit pulses across multiple symbol intervals
- This dispersion of pulses causes inter-symbol interference (ISI) where one symbol interferes with adjacent one
- Eventually leads to bit error rates (BER)





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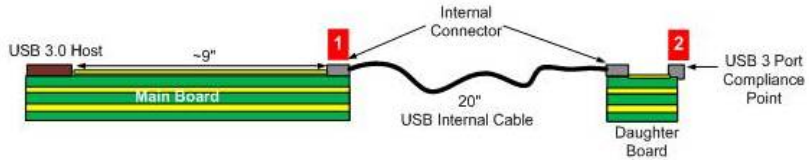
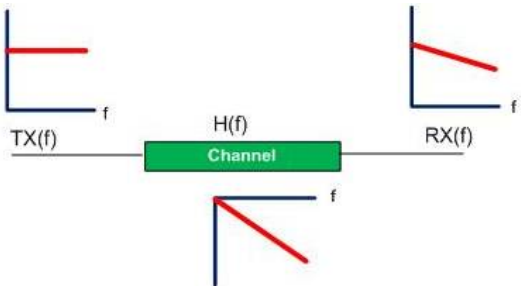
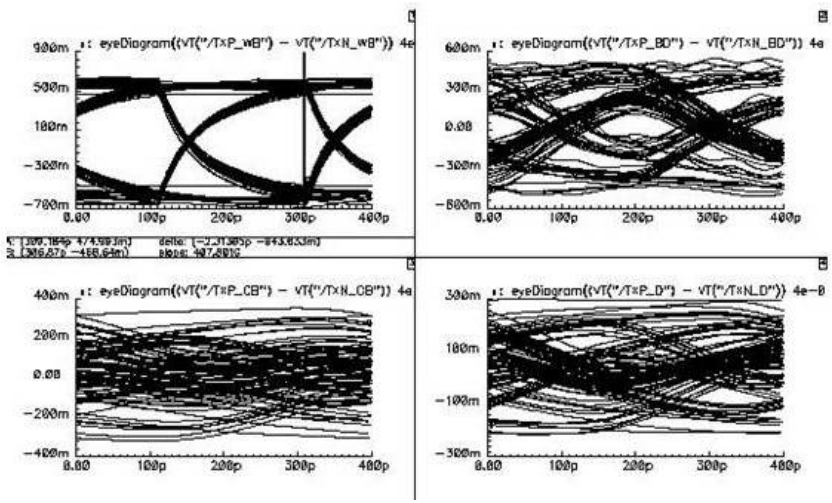
How bad is it?

- In many applications, such as implementation of a USB 3.0 port in the front panel of a desktop PC, the SueprSpeed signals are routed over the host board as well as the internal USB 3.0 cable and daughter card
- This channel can be modeled as a low-pass filter with a transfer function that exhibits high frequency loss.
- Equalizers (with high–frequency gain) are used to counteract the loss the signal encounters in the channel
  - Ideal Scenario:
    - If E(f), the transfer function of an equalizer is tuned to be equal to 1/H(f). Then RX(f) will be equal to TX(f)
  - Practically, this is not possible as equalizers amplify high-frequency signals, but also amplify noise
- USB 3.0 requires that continuous time linear equalizer (CTLE) function be applied to the received signal in order to open the eye
  - For many cases, the high-frequency loss and jitter are so severe that it is not possible to get an open eye after a 3m USB 3.0 cable.
- This shows a simulation based on the channel shown
  - The eye is completely closed – even after the CTLE function is applied
  - This results in a bit error in the actual data transmission.
- Redrivers are increasingly being used in PC and server platforms to compensate for frequency dependent losses in the channel media.







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High-Speed (2.0) Differential Routing

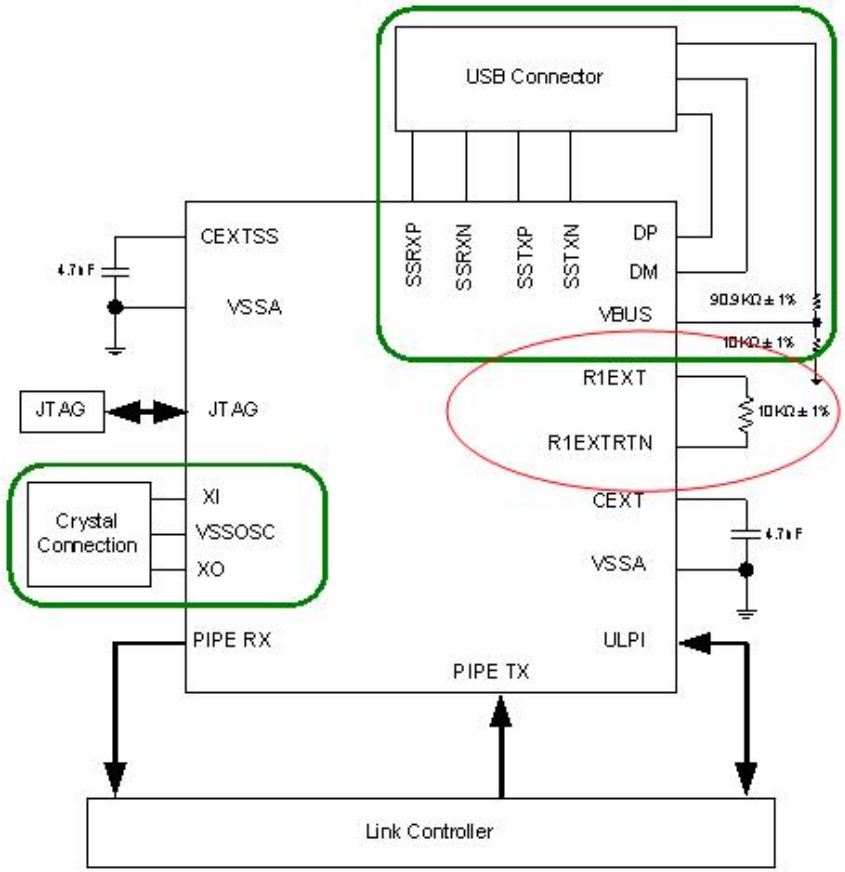
- Differential pair (D+/D–) connected to a USB connecter.
  - Type A
  - Type B
  - Mini/Micro
- Should be routed with 90 ohms +/-15% differential impedance.
- Should be trace length matched.
  - Max trace length mismatch between High speed USB signal pairs should be no greater than 150 mils.
  - Keep total trace length to a minimum.
- Route differential traces first.
  - Route the differential pairs on the top or bottom layers with the minimum amount of vias possible.
- No termination or coupling caps are required.
- If a common mode choke is desried, then place the choke as close as possible to the USB connector signal pins.
- Likewise ESD clamps should also be placed as close as possible to the USB connector signal pins (closer than the choke).

Multi-Gbps Differential Routing

- Consists of two differential routing pairs
  - a transmit pair (TX)
  - a receive pair (RX)
- Each diff pair traces should be routed with differential impedance
  - SuperSpeed USB 90 ohms +/-15%
  - SATA 100 ohms +/-15%
  - PCIe 100 ohms +/-15%
- Max trace length mismatch between SuperSpeed USB pairs should be no greater than 2.5 mils.
  - The TX pair does not have to be the same length as the RX pair.
  - Keep total trace length to a minimum.
- Route differential traces first.
  - Route the differential pairs on the top or bottom layers with the minimum amount of vias possible.
- The TX pair requires 0.1uF coupling caps for proper operation.
  - The package/case size of these caps should be no bigger than 0402.
  - C-packs are not allowed.
  - The caps should be placed symmetrically as close as possible to the USB connector signal pins.
- If a common mode choke is desired then place the choke as close as possible to the USB connector signal pins (closer than the transmitter caps).
- Likewise ESD clamps should also be placed as close as possible to the USB connector signal pins (closer than the choke and transmitter caps).

Calibration Resistor

- **Connect 1% 10k calibration resistor between R1EXT and R1EXTRTN.**
- **Place within 500 mils of the device.**



Power Considerations

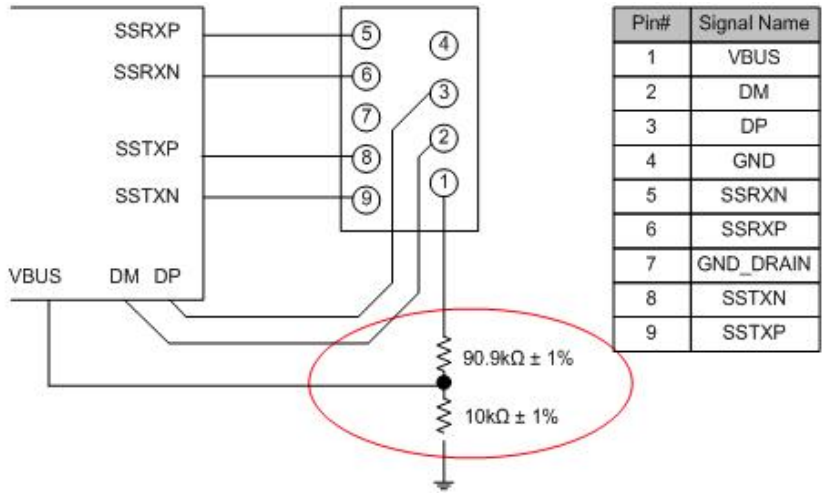
- All supplies must have 0.1-uF bypass capacitors to ground in order for proper operation.
  - VSSA = Analog Supply (1.1V, 1.8V and 3.3V) Ground
  - VSS = Digital Supply (1.1V and 1.8V) Ground
  - VSS and VSSA can be connected together to form one ground plane.
    - This technique allows for creating a large image plane for the signal layer directly adjacent to the ground plane.
- One capacitor for each power terminal.
- Place the capacitor as close as possible to the terminal on the device and keep trace length to a minimum.
- Smaller value capacitors like 0.01-uF are also recommended on all supply terminals.
- Capacitor Selection Recommendations
  - Bypass capacitors are recommended to be X7R-type
  - Bulk capacitors: Low-ESR specifications are recommended to minimize low frequency power supply noise.

Power-Up/Down Sequencing

- **Absolute maximum power terminal ratings must not be exceeded to prevent damaging the device.**
- **There is no requirement on which power rail be applied first as long as RESET is held active.**
  - **RESET should be held until power rails reach their minimum value**
- **Also, it does not matter which rail is removed first.**
- **View the respective implementation guides for recommended TI power supply devices.**

USB VBUS

- **VBUS is a 5-V source that is connected via a voltage divider.**
- **For TI devices, connect a 90.9K 1% resistor from the cable VBUS connector to the USB VBUS terminal and a 10K 1% resistor from USB VBUS to ground.**



Pin#	Signal Name
1	VBUS
2	DM
3	DP
4	GND
5	SSRXN
6	SSRXP
7	GND_DRAIN
8	SSTXN
9	SSTXP

VBUS: Polyfuse vs. Power Switch

USB Switches vs. Polyfuses

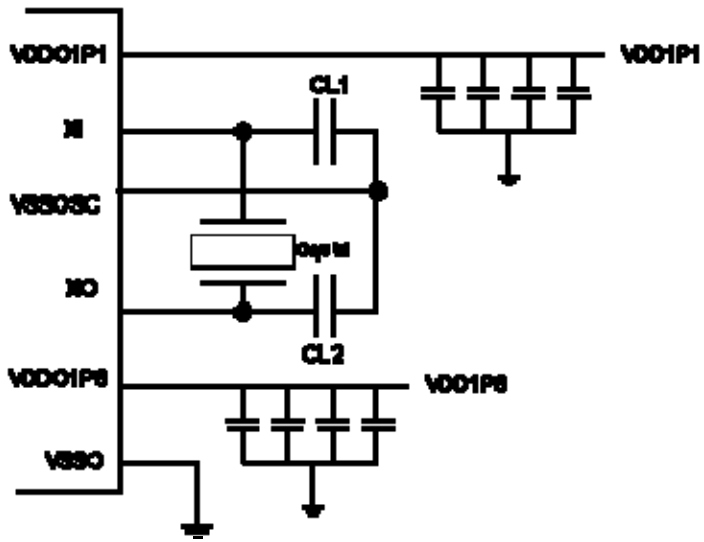
Feature	Polyfuse	USB Switch
Report Over-current Condition	NO	YES
*Fast Response Time	~15ms	~2µs
Limit Output Current < 5A	YES	YES
Meets VDROP Requirements (80mV)	2.5A Device	YES
Enabled/Disabled by Controller	NO	YES
Controlled rise/fall times?	NO	YES
Under Voltage Lockout?	NO	YES
*Wears out after repeated faults?	Yes	No
*Meet Safety Requirements (i.e. UL?)	Yes	Yes
Blocks reverse current when off?	No	Yes

Limiting Inrush Current on VBUS

- Inrush current can occur on VBUS when a function is plugged into the network.
  - Inrush is tested during USB compliance testing
- If the design is Bus Powered, use of the TI TPS2560/61 is recommended.
  - These can be used to power both downstream USB ports as well as SATA ports
- For example
  - The bulk capacitance used to supply power to a peripheral device can be quite large, causing inrush current when the USB cable is connected.
  - The TPS2560/61 power-distribution switches are intended for applications where heavy capacitive loads are likely to be encountered.

Input Clock

- TI's SS USB devices support an either an external oscillator source or a crystal unit
  - Selectable via strap pin or register
  - Crystal
    - Since XI and XO are coupled to other leads and supplies on the PCB, it is important to keep them as short as possible and away from any switching leads.
    - It is also recommended to minimize the capacitance between XI and XO.
      - This can be accomplished by connecting the VSSOSC lead to the two external capacitors CL1 and CL2 and shielding them with the clean ground lines.
    - The VSSOSC should not be connected to PCB ground.
  - Clock Oscillator
    - If a clock is provided to XI instead of a crystal, XO is left open.
    - Clock needs to be 1.8V.
    - VSSOSC is connected to the PCB ground plane.
- The reference clock frequencies are selectable for most devices.



Input Clock Jitter Tolerance

- **Reference clock jitter is an important parameter.**
- **Jitter on the reference clock will degrade both the transmit eye and receiver jitter tolerance no matter how clean the rest of the PLL is, thereby impairing system performance.**
  - **Additionally, a particularly jittery reference clock may interfere with PLL lock detection mechanism, forcing the Lock Detector to issue an Unlock signal.**
- **A good quality, low jitter reference clock is required to achieve compliance with supported USB3.0 standards.**
  - **PLL's typically have a number of additional jitter components, thus the Reference Clock jitter must be considerably below the overall jitter budget.**

ESD Protection

- **TI's USB devices provide ESD protection on all signal and power pins**
  - **Up to 2000-V using the human body model.**
  - **500-V using the charged device model.**

- **If more protection is desired, TI has a wide selection of integrated protection devices that meet the SuperSpeed USB standards and:**
  - **Meet or exceed IEC61000-4-2 (Level 4) requirements.**
  - **Can be used on any of the differential pairs**
  - **Place the device as close as possible to the signal pins of the connector.**
  - **Refer to the datasheet for more information regarding the selected device.**

USB Product Portfolio

Transceivers

TUSB1105/1106
USB Full-speed
NXP Drop-in Replacement

TUSB2551A
USB Full-speed
Micrel Drop-in Replacement

Peripherals

TUSB3210
USB Full-speed
General Purpose 8052 MCU

TUSB3410
USB Full-speed
Programmable USB-to-Serial Bridge

TUSB6250
USB High-speed
Programmable USB-to-IDE Bridge

Hub Controllers

TUSB2036
USB Full-speed
2/3-Port Configurable

TUSB2046B
USB Full-speed
4-Port

TUSB2077A
USB Full-speed
7-Port

TUSB2136
Compound USB Full-speed 2-port with
General Purpose 8052 MCU

Hosts / On-the-Go

TUSB6020
USB High-speed OTG
VLYNQ Local Bus Interface

Full/Low/High-Speed Enabled Devices

SuperSpeed Enabled Devices

TUSB1310
USB 3.0 Transceiver

TUSB1310A
2nd Gen USB 3.0 Transceiver

TUSB9260
USB 3.0 to SATA (3Gbps)

TUSB9261
2nd Gen. USB 3.0 to SATA (3Gbps)

TUSB8040
USB 3.0 4–port Hub

TUSB7340
USB 3.0 4–Port xHCI

TUSB7320
USB 3.0 2–Port xHCI

USB 3 Re–Driver

SN65LVPE502 & 502CP
USB 3.0 1 Channel Re-Driver w/ EQ

New Production Release

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SN65LVPE502 & SN65LVPE502CP:
Single Lane Re-Driver w/ EQ & DE

Features

- Selectable Input Equalization (0/7/15db)
- Selectable Output De-emphasis

LVPE502 DE Selection

DEx*	OSx* NC	0	1
NC	-3.5dB	-2.2dB	-4.4dB
0	-6.0dB	-5.2dB	-6.0dB
1	-8.5dB	-8.9dB	-7.6dB

LVPE502CP DE Selection

DEx*	OSx* NC	0	1
NC	0	0	0
0	-3.5dB	-2.2dB	-4.4dB
1	-6.0dB	-5.2dB	-6.0dB

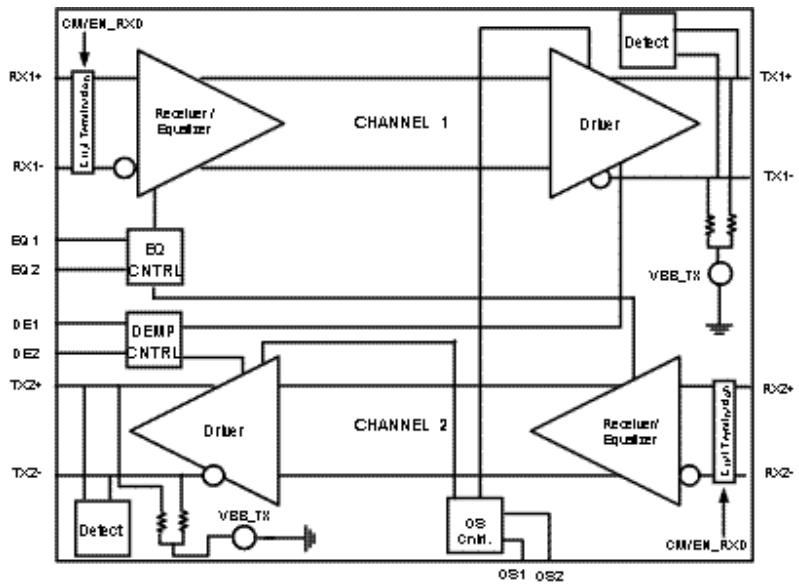
- Low Power
  - 315mW typical active power (U0)
  - 70mW typ. Power in U2/U3 mode
  - 7mW typ. power with disconnected cable
- Excellent jitter and loss compensation
- 4mm x 4mm, 24–QFN Package
- High protection against ESD transient
  - 8KV HBM & 1.5KV CDM

Applications

- PC Motherboards
- PC Docking Stations
- PC Add–in Cards
- Backplane & Cabled applications

Benefits

- Makes bad signals good again
- Flexible signal conditioning for different media
- Extends battery Life
- Up to 40 inches of 4 mil stripline on FR4
- Save board space
- Protection against transients



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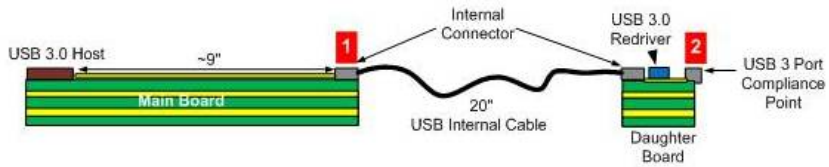
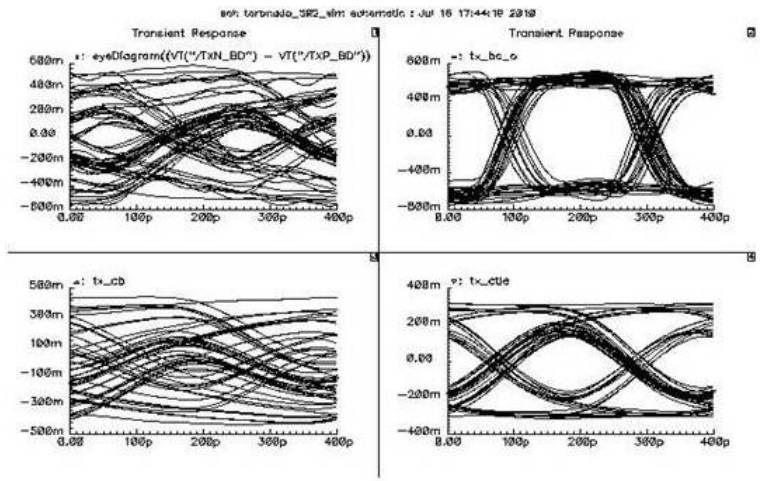
How can these help?

- **In its most basic form a redriver is required to compensate for high-frequency losses.**
  - **Programmable high-frequency gain, E1(f), to the input signal**
  - **Pre-emphasize signal at transmitter E2(f)**
  - **Both E1(f) and E2(f) act to lower (E1(f)*E2(f)) the affect of high-frequency losses H(f).**
  - **In a USB 3.0 link, it also must be:**
    - **Compliant with the USB 3.0 electrical specification**
    - **Support receiver detection**
    - **Be fully transparent to the out-of-band signal like low-frequency periodic signal that is used to communicate link state machine status between host/hub and end device.**
- **USB 3.0 compliance eye diagram with reference to front panel implementation (shown above).**
  - **The main difference is that a USB 3.0 redriver used at the front panel port results in a fully open eye even with a 3m cable**





SuperSpeed USB 3.0 Analog PHY

Features

- ***Superior RX sensitivity*: < 50 mV peak to peak differential**
  - **Twice as good as required by USB 3.0 specification**
- **Integrated Fractional PLL supporting multiple reference frequencies**
- **Integrated Spread Spectrum Clock functionality**
- **Best–in–class Adaptive Equalizer & Multi-tap de-emphasis**
- **Integrated into 65 nm technology**
- **Internal polarity inversion**
- **IEEE1149.1 JTAG and IEEE1149.6 ACJTAG**
- **Hot Plug compliant**

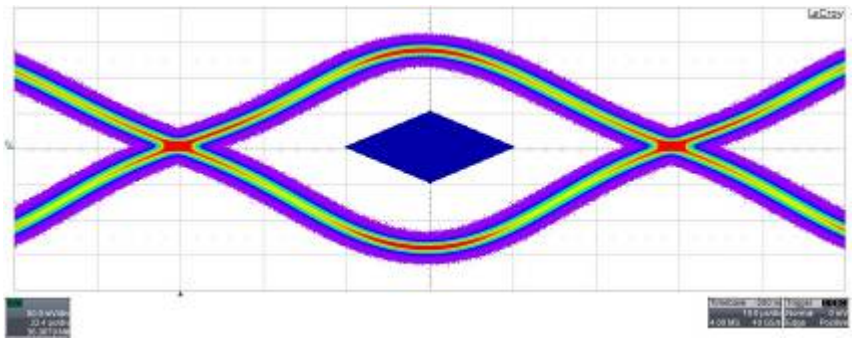
Benefits

- **Enables signal detection even with weak signal transmission**
- **Cost savings enabled by reuse of existing system clocks**
- **Reduce BOM costs by requiring low-cost crystal input only**
- **Autotunes RX performance allowing for simpler board layout and longer cable usage**
- **Best in class area and performance**
- **Ease board design**
- **Allows cost effective structural testing of loaded PCB**

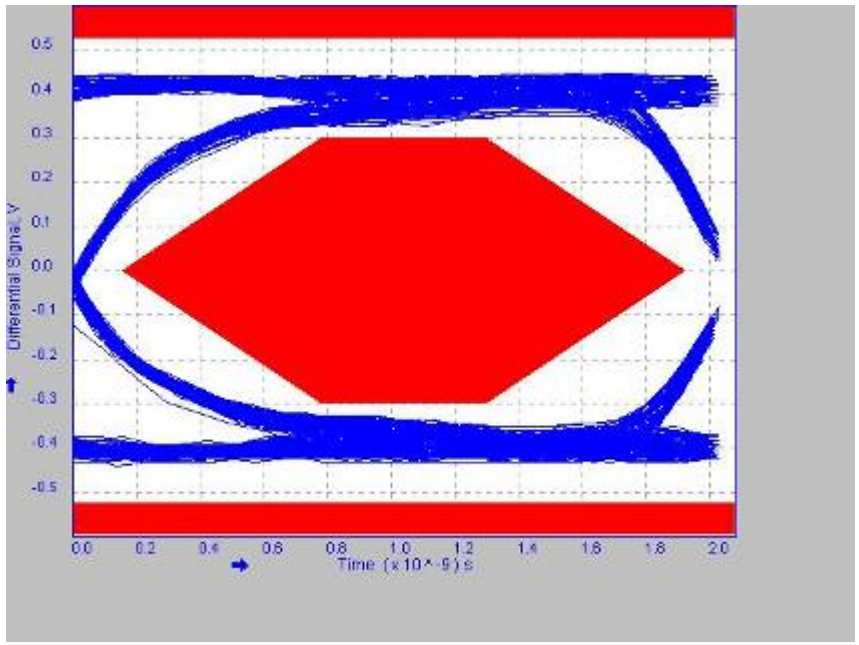
Key technology enabler for all SuperSpeed USB 3.0 Products

Eye Diagrams

SuperSpeed



USB 2.0 High–Speed



TUSB1310A:
Discrete SuperSpeed Phy

Features

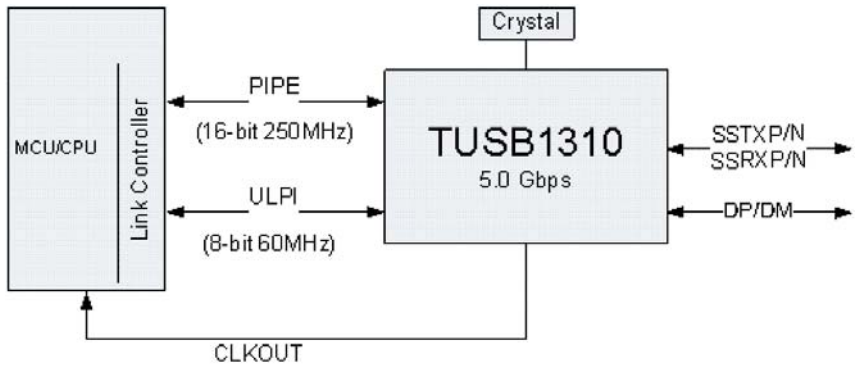
- USB Interface
  - USB 3.0 PHY for SuperSpeed signaling
  - USB 2.0 PHY for high-speed, full-speed, and low-speed signaling
- Digital Interface
  - PIPE3 For SuperSpeed signal path
  - ULPI for high-speed, full-speed, and low-speed signal path
- Performance enabled by TI's Leading *SuperSpeed USB Analog PHY Technology*
- 175–ball, 12x12, 0.8mm, BGA

Benefits

- Supports all USB application spaces
- Industry standard interface enables easy system integration with attached core
- Class leading performance measured by USB–IF Electrical Compliance Testing

Applications

- FPGA Digital Core Implementation
- High–resolution Imaging
- Test Equipment



Typical Application

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TUSB1310A Digital Interfaces

Signal Name	Type
TX_CLK	TX
TX_DATA[15:0[	TX
TX_DATAK[1:0]	TX
PCLK	RX
RX_DATA[15:0]	RX
RX_DATAK[1:0]	RX
RX_VALID	RX

- **PIPE Interface**
  - **1.8V LVCMOS.**
  - **Source synchronous signals for each direction of the interface should be matched in length:**
    - **To within 250 mils.**
  - **Other signals can be of different lengths but should be as short as possible.**
  - **External source series termination resistors are not required IF:**
    - **The interface is kept to less than two inches in length**
    - **With an impedance of 50 Ohms +/-10%**
  - **Routing this interface longer than two inches or through a connector is not recommended.**
    - **If this must be done, special care must be taken to select the proper high-speed connector as well as modeling of the transmission line.**
  - **Post route modeling of the circuit is recommended.**
- **ULPI Interface**
  - **1.8V LVCMOS.**
  - **They should be as short as possible and matched in length**
    - **With a single ended impedance of 50 Ohms +/-10%**

TUSB1310A

- **FPGA Timing**
  - **FPGA must have an IO timing capability of 250 MHz.**
  - **Use PIPE and ULPI timing parameters as defined in the data sheet.**
  - **Anticipate several iterations of FPGA builds in order to tweak the PIPE and ULPI signals relative to the clock in order to meet the AC characteristics**
- **General Layout Guidelines**
  - **Use appropriate high speed logic analyzer connectors on the PIPE and ULPI interfaces for initial prototypes is encouraged.**
    - **Especially useful for FPGA prototyping.**
  - **CEXT and CEXTSS (balls A14 and M14) are repurposed on the TUSB1310A vs TUSB1310. Check the appropriate data sheet for the revision you are using.**

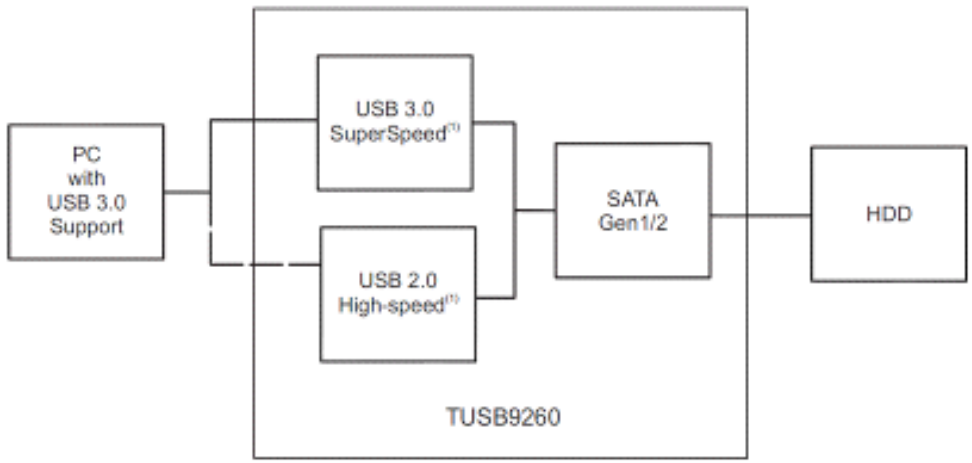
TUSB9261:
USB to SATA 3–Gig Bridge

Features

- USB Interface
  - Certified as compliant by the USB Peripheral Interop Lab: TID#340730020
  - SuperSpeed, High–speed, & Full–speed support
  - Multiple Protocol Compliant:
    - Attached SCSI Protocol (UASP)
    - Mass Storage Class Bulk-Only Transport
    - HID Class
    - Firmware Update support
- SATA II Interface
  - 1 Port, SATA 2.6 compliant:: Gen1i, Gen1m, Gen2i, Gen2m
  - Hot Plug Support
- Performance enabled by TI's Leading *SuperSpeed USB Analog PHY Technology*
- Up to 12 GPIOs
  - 2 GPIOs have PWM functionality for LED control

Benefits

- Ultra Fast Sync-and-Go User Experience
- Cross Platform Compatibility & Interoperability with latest high-performance storage drives
- Class leading performance measured by USB–IF Electrical Compliance Testing
- Enables customer defined end-user configuration



Applications

- External HDDs
- External Optical Drives

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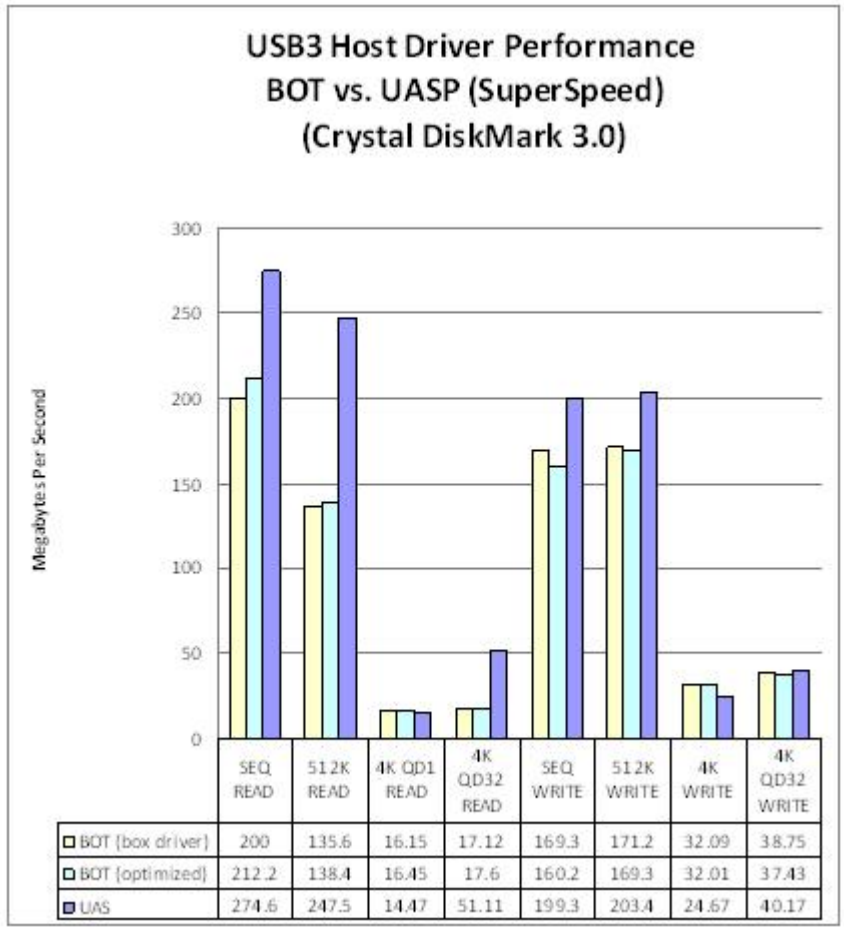
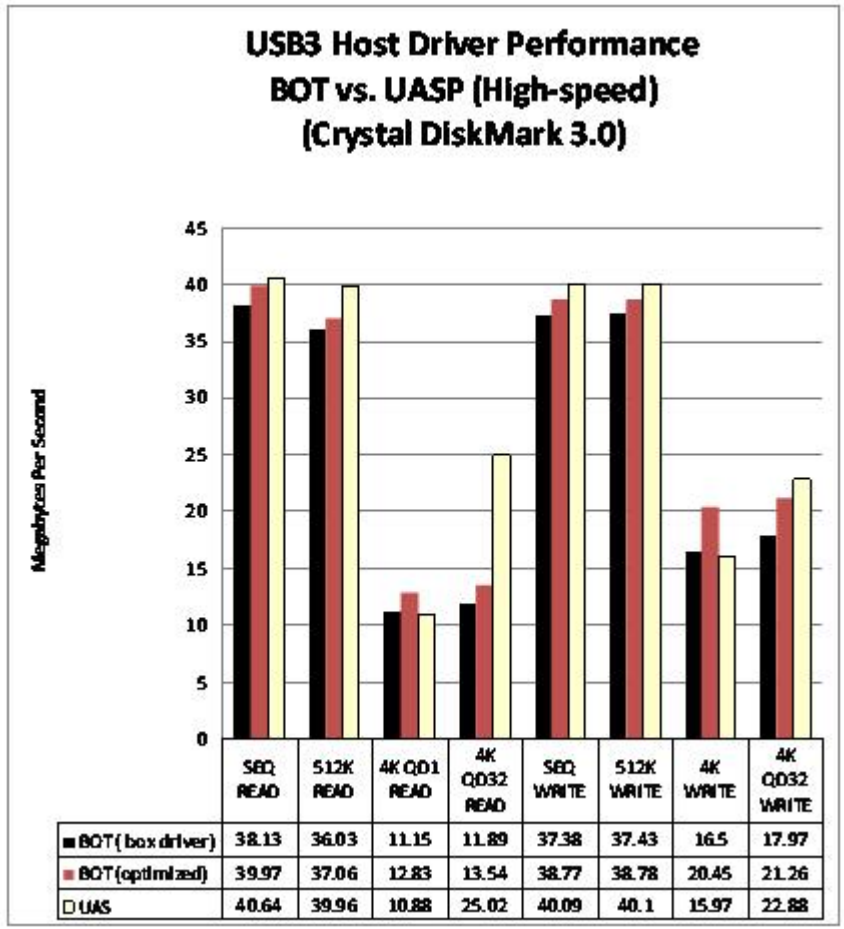
UASP SuperSpeed Performance Comparisons

- UAS benefits performance more pronounced for both read and writes with SuperSpeed
  - Maximum read performance reaching disk transfer limits
  - Benefits from lower bus protocol overhead for SuperSpeed and lower latency between commands for UASP
- Small transfers receive large performance gains with UAS queuing
  - Nearly 200% performance increase for 4 KB read with queue depth of 32
  - Small penalty when queuing not enabled due to protocol overhead, but latency between command execution greatly reduced.
- Test Configuration
  - USB 3.0 SSD
    - TUSB9260 with Intel X25-E SSD
  - Host Stack
    - NEC xHCI with MS BOT (box driver)
    - TI xHCI with optimized BOT
    - TI xHCI with UASP



UASP High-speed Performance Comparisons

- Small performance gains for large transfers
  - Reaching limits due to USB High-speed transfer rates and bus overhead.
  - Benefits greater compared to non-optimized BOT transfers
- Large performance for small transfers with queuing
  - More than 100% performance increase for 4 KB reads over standard BOT
  - Small penalty when queuing not enabled due to protocol overhead, but latency between command execution greatly reduced.
- Test Configuration
  - USB 3.0 SSD
    - TUSB9260 with Intel X25-E SSD
  - Host Stack
    - NEC xHCI with MS BOT (box driver)
    - TI xHCI with optimized BOT
    - TI xHCI with UASP



TUSB8040:
SuperSpeed USB 4–port Hub

Features

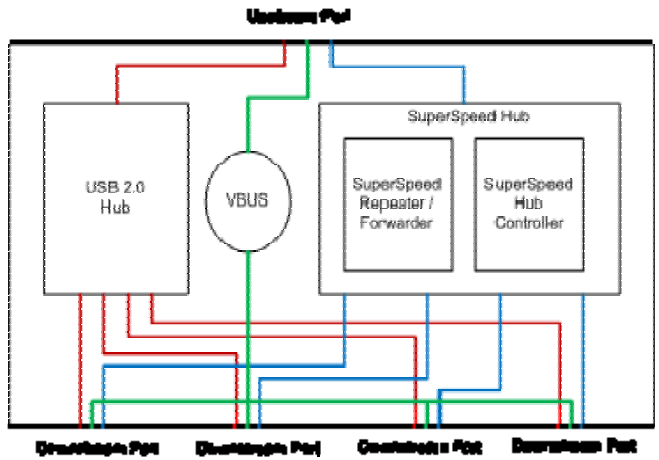
- Supports all USB speeds
  - USB 2 Hub Logic includes Transaction Translators (TTs) for FS/LS support
- Performance enabled by TI's Leading *SuperSpeed USB Analog PHY Technology*
- VBUS input allows control of integrated USB 2.0 termination pull–up
- 80–pin HTQFP, RoHS compliant package
  - *100–pin QFN in development*

Applications

- Discrete Hub Boxes
- Hub in Monitors
- Embedded USB Ports
- Hub on Motherboard/Front-panel for Desktop/Notebook PCs

Benefits

- Increased number of available USB Ports
  - Interoperability with latest high-performance USB Peripherals
  - Full backwards and forward compatibility of all ports in a system
- Class leading performance measured by USB–IF Electrical Compliance Testing
- Eliminates need for external circuitry reducing implementation cost
- Flexible options to meet application requirements



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TUSB8040 Functionality

- **Ganged port power management and over current**
  - *Future 100 pin versions will enable per port power management and over current inputs*
- **Optional serial EEPROM or SMBus**
  - **Allows custom VID/PID and Manufacturer and Product Strings**
  - **See table for programmable features**
- **Unique product serial # for each device is generated from the on–chip 48–bit Die ID.**
- **Supports USB charging port applications compliant to USB Battery Charging 1.1**
- **Downstream ports can be independently**
  - **Enabled or disabled**
  - **Marked as removable or permanently attached**
- **Hub status outputs**
  - **High-speed suspended**
  - **High-speed operation**
  - **SuperSpeed suspended**
  - **SuperSpeed operation**
- *Optional USB 2.0 port indicators supported in future 100 pin package option*

Package Option:	80 pin QFP: PFP		*100 pin QFN: RKM*	
Configuration Option:	EEPROM	Pin Strap	*EEPROM*	*Pin Strap*
Per port usage (Enable/Disable)	✓		✓	✓
Per port removable/permanently attached device	✓		✓	✓
Per port USB battery charging 1.1 support	✓		✓	✓
Ganged or per port power switch and over current inputs	**Ganged only**		✓	✓
USB 2.0 port indicator support			✓	✓
Custom VID/PID	✓		✓	
Custom product, manufacturer, and serial number strings	✓		✓	

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TUSB8040 vs. Comp.

Feature	Comp.	TI	TI Advantage
Better Analog Performance	Reduced SS Eye Margin HS Eye Mask failure & 3X Jitter	Better Performance (See following Eye Diagrams)	Less likelihood of interoperability and connection issues over longer trace lengths, poor connectors, and longer cables
Package	88 pin QFN (10x10)	80 pin QFP (14x14) 100 pin QFN (9x9) <In Development>	Multiple package options & smaller footprint to support a broader range of applications
BOM Cost	Requires external 512K EEPROM	EEPROM not required, but is optional for custom VID/PID	Lower cost option by eliminating EEPROM
Hot Plug Enumeration	Testing of various released devices shows a consistent failure to enumerate 100% of Hot Plug insertions	Reliable Hot Plug Enumeration	Consistent interoperability results
1) USB 3 Remote Function Wakeup 2) USB 2 ECN for LPM Support 3) Support BOS Descriptors for both HS and SSt	1) Not Supported 2) Not Supported 3) Supported on SS Only	1) Supported 2) Supported 3) Supported on HS & SS	Full support as required by the USB Standard

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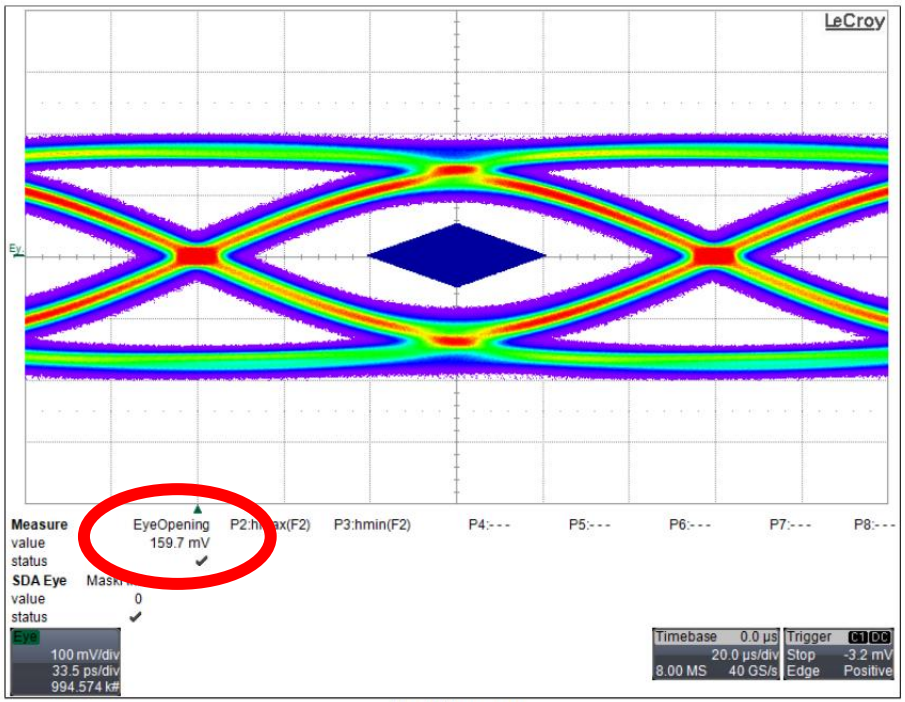
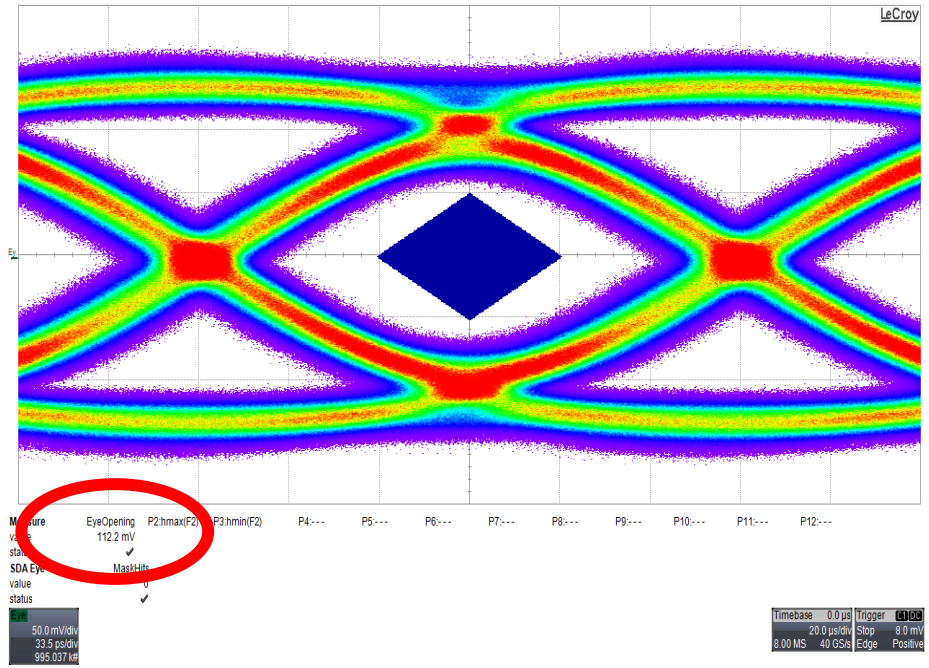
SuperSpeed Eye Comparison

TI TUSB8040



Eye Diagram

Competitor



- **TI shows a > *42%* wider eye opening at SS.**
  - **TUSB8040: 159.7mV**
  - **Comp: 112.2mV**

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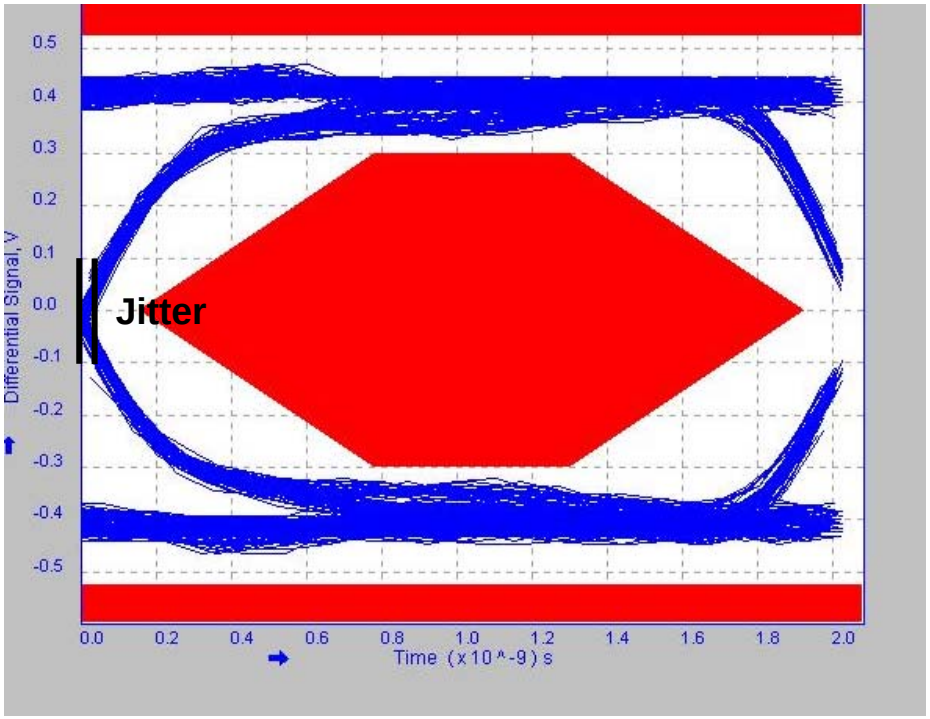
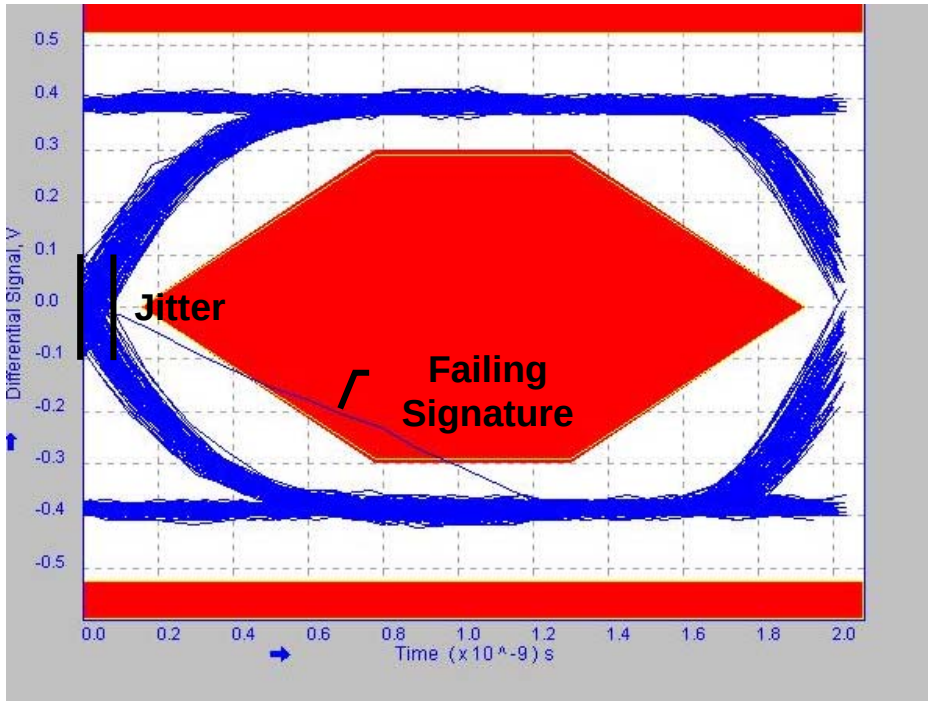
USB2.0 Eye Diagram

TI TUSB8040



Competitor



- **Comp eye diagram tests show a failing signature which crosses the eye mask on all upstream and downstream ports**
  - **This could be a design flaw which may cause interoperability problems**
- **Comp eye diagram also shows approximately 3X the jitter**
  - **While passing the eye masks tests this could limit functionality when used in systems with long traces or cables – possibly limiting maximum trace lengths**

USB–IF Hub Certification Status

- As of May–2011, there is not a SuperSpeed HUB Certification Program available from the USB–IF.
  - USB–IF Schedule is by end of 2Q11
- When one comes available, the first step will be to certify as a USB 2.0 compliant hub.
  - The TUSB8040 is the first (and only to date) SuperSpeed hub that has passed USB 2.0 certification testing
    - As shown on the previous page, the VL810's HS eye diagram prevents it from being able to achieve this certification.
- The USB–IF Peripheral Interoperability Lab is presently utilizing the TUSB8040 to develop the SuperSpeed Compliance Program

TUSB7320 & TUSB7340:
PCIe-based xHCI Controllers

Features

- x1 PCIe Gen II to SuperSpeed xHCI Host Controller
  - Compliant to xHCI 0.96 Specification
  - Options for both 2 Port (TUSB7320) and 4 Port (TUSB7340)
    - Adjustments for transmit strength and de-emphasis for connection to a local device
    - Can be Independently enabled/disabled
    - Independent power control and overcurrent detection
- Full hardware solution – No external FLASH
- Pin Compatible between 2 Port & 4 Port Options
- USB Legacy Support
- x1 PCIe Gen II Interface
  - Supports CLKREQ# protocol
- Performance enabled by TI's Leading *SuperSpeed USB Analog PHY Technology*
- Optional EEPROM interface for loading initial configuration information for non-Motherboard Applications
  - Can also be loaded via PCIe config writes

Benefits

- Enables platforms to support newest USB Standard (USB 3 / SuperSpeed)
  - Satisfies Microsoft WHQL Requirements
  - Support for varying Port Count Requirements
  - Flexible Port Configuration Options
- Saves up to $0.20 in BOM cost.
- Flexible Board design offering multiple SKU options
- BIOS support for USB boot
  - Keyboard, mice, USB drive
- Compatibility with industry standard system expansion bus
- Class leading performance measured by USB–IF Electrical Compliance Testing

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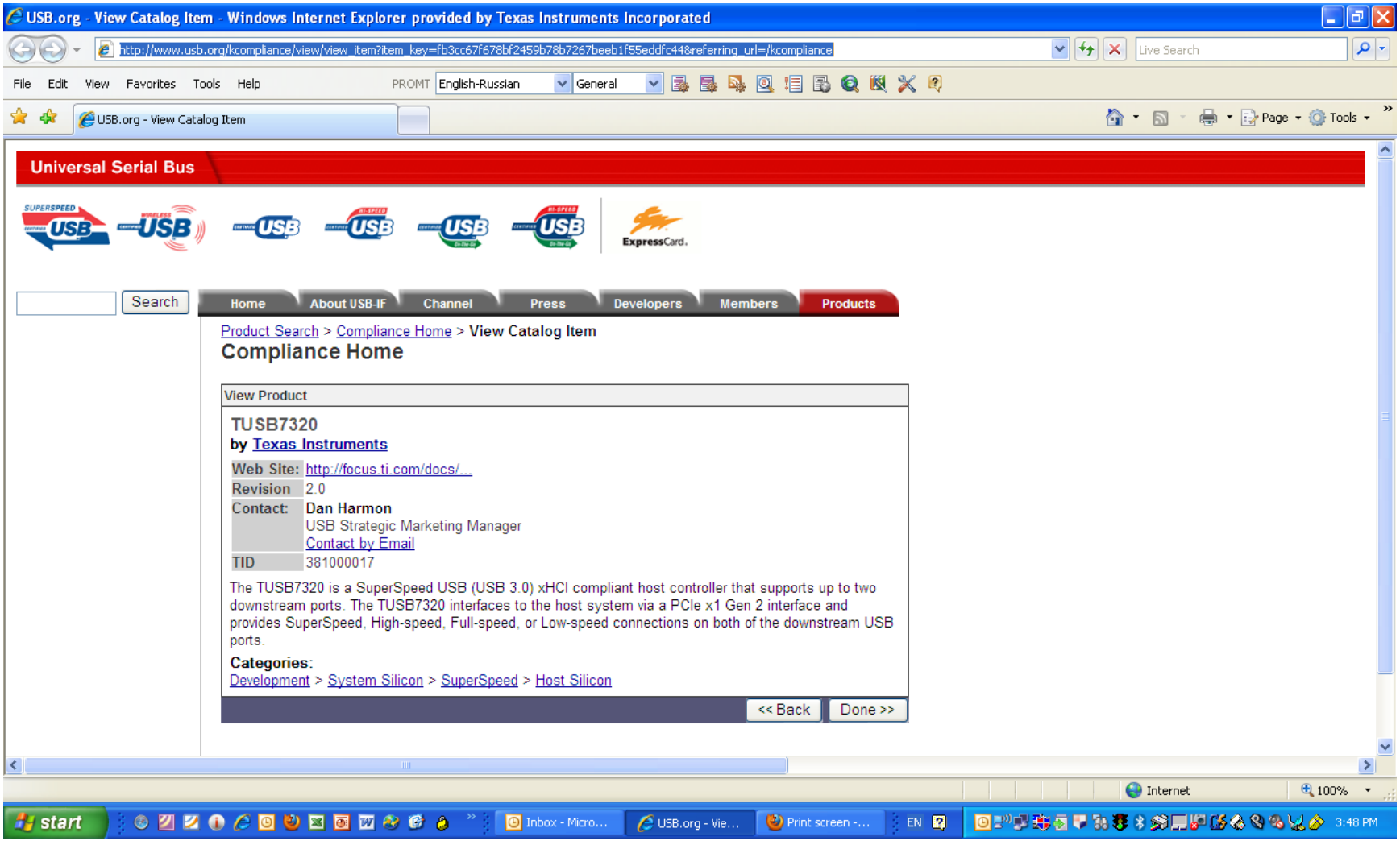
TUSB7320

USB–IF Certified 2-Port Host Controller



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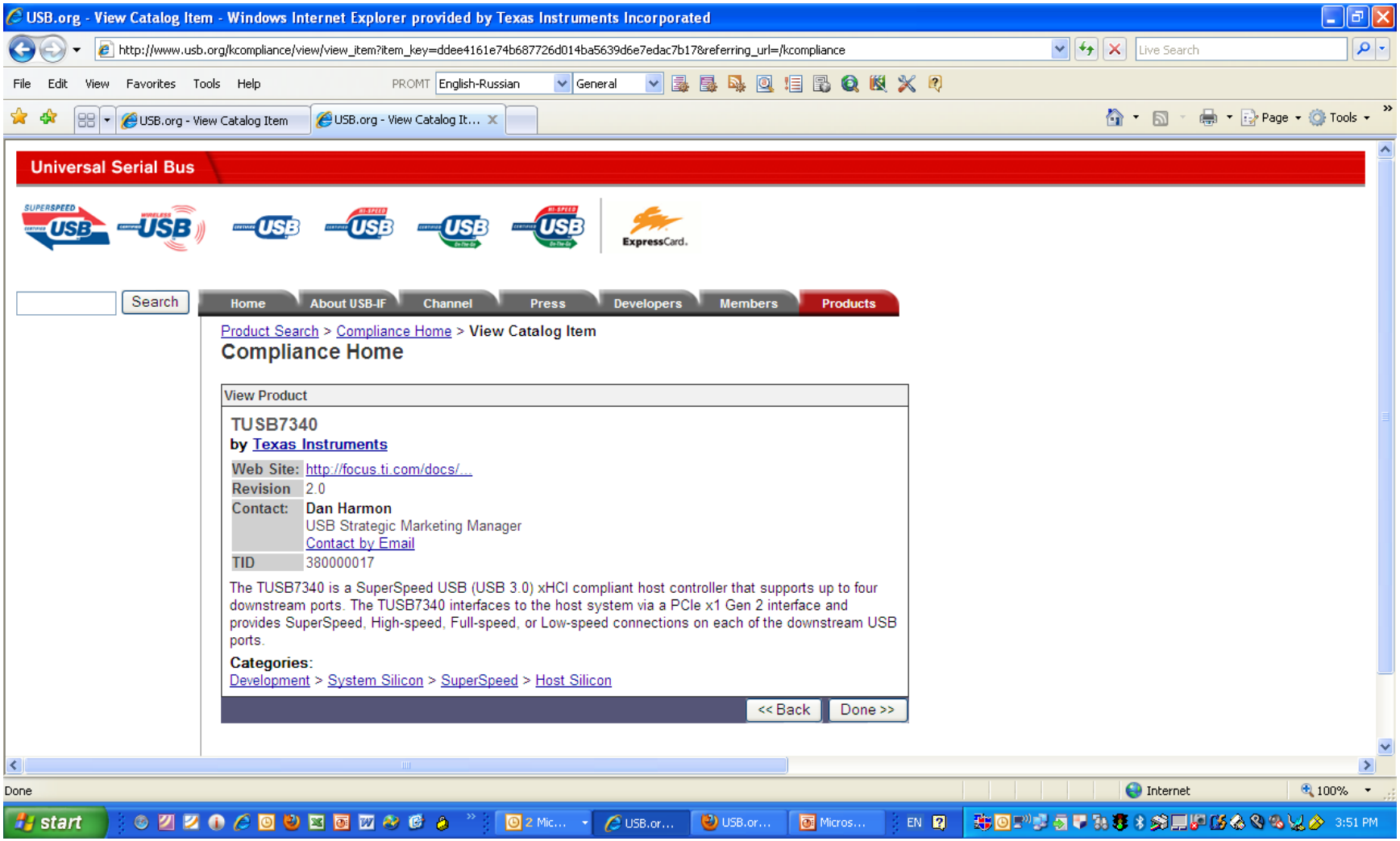
TUSB7340

USB–IF Certified 4-Port Host Controller



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Comparison to Closest Competitor

Feature	Competitor	TI	TI Advantage
# of Ports	**2-port Only**	**Choice of 2 and 4 ports** **TUSB7320 – 2 Port** **TUSB7340 – 4 Port**	Footprint compatible option for 2 and 4 Port Implementations. **Saves cost of additional USB Hub to support 4 Port Implementations.**
Suspend Power	**~500mW**	**<100mW**	Saves battery life
Package	**10x10 BGA**	**9x9 PWQFN**	Smaller foot print + No External EEPROM/Flash Chip
BOM Cost	**Requires Flash/EEPROM**	**Optional; only for custom settings.**	Estimated savings of $0.10-0.20 with TI host
	Fixed 24MHz Crystal	**Any frequency between 20MHz-50MHz**	**•TI host allows use of 48MHz clk typically available in most system** • Estimated savings of $0.20-.30
	UAS support for mass storage not enabled by default (royalty $$ based)	**UAS support for mass storage enabled by default (see next slide)**	**• No need to pay royalty to enable UASP support, saves up to $0.50** • Improved performance
Spread Spectrum Clocking (SSC)	**Not compliant to USB 3.0 spec (center spreading)**	**Compliant (down spreading)**	**USB3 device can have SSC enabled when used with TI host.** Reduces the maximum EMI emission.
Performance	**The TUSB73x0 wins three-out-of-four direct performance comparisons. Both single and multi-port concurrent write performance is significantly better at 37% and 15% respectively. Multi-port concurrent-read performance lags behind the competition by 7.5%. See folloing slides for details**		

Compared to its closest competition, TI HOST delivers a lower BOM implementation with up to $1.00 in estimated savings, while providing a compliant solution.

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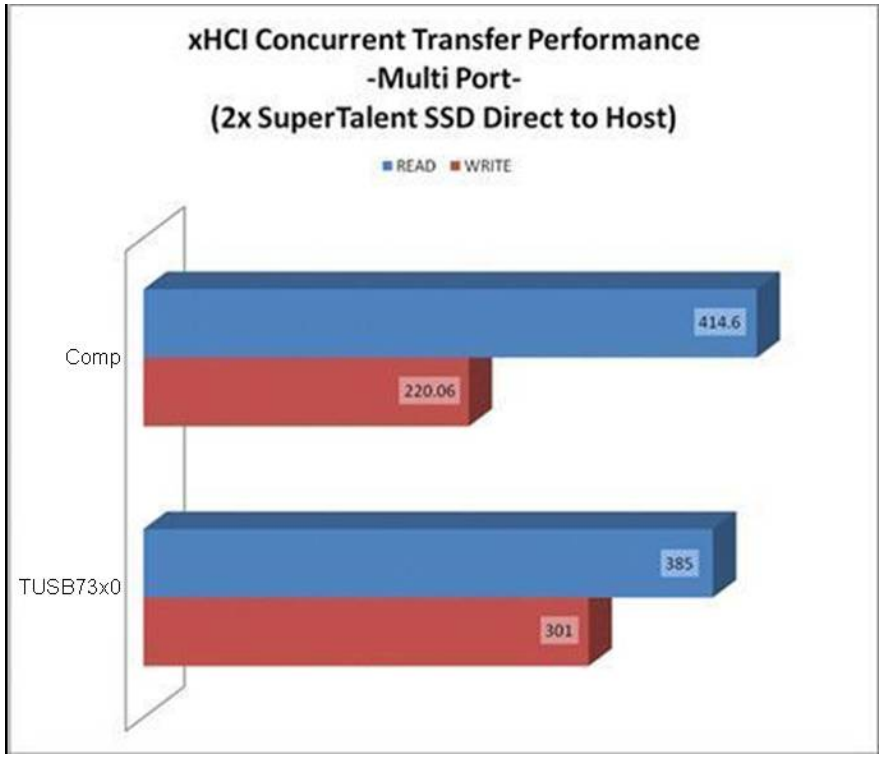
Performance Comparison

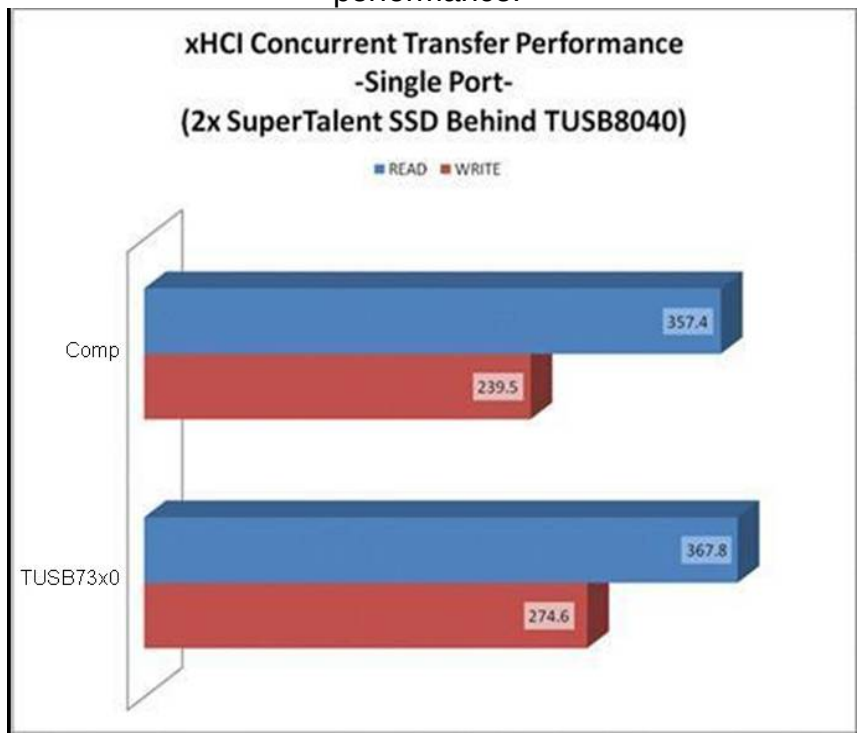
Test Case #1

Plug 2x SuperTalent SSDs directly into host and measure concurrent performance.



Test Case #2

Plug 2x SuperTalent SSDs directly into a single host port via the TUSB840 hub and measure concurrent (behind hub) performance.



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Support Files

- IBIS
- BSDL
- Reference Design
- Gerbers and Layout Files
- All available on TI website

For More Information

- **TI E2E Online Community: e2e.ti.com**
- **General questions on USB devices:**
  - **usb@ti.com**
- **Consumer & Computing Product Marketing**
  - **dharmon@ti.com**

Questions

Thank you for your time